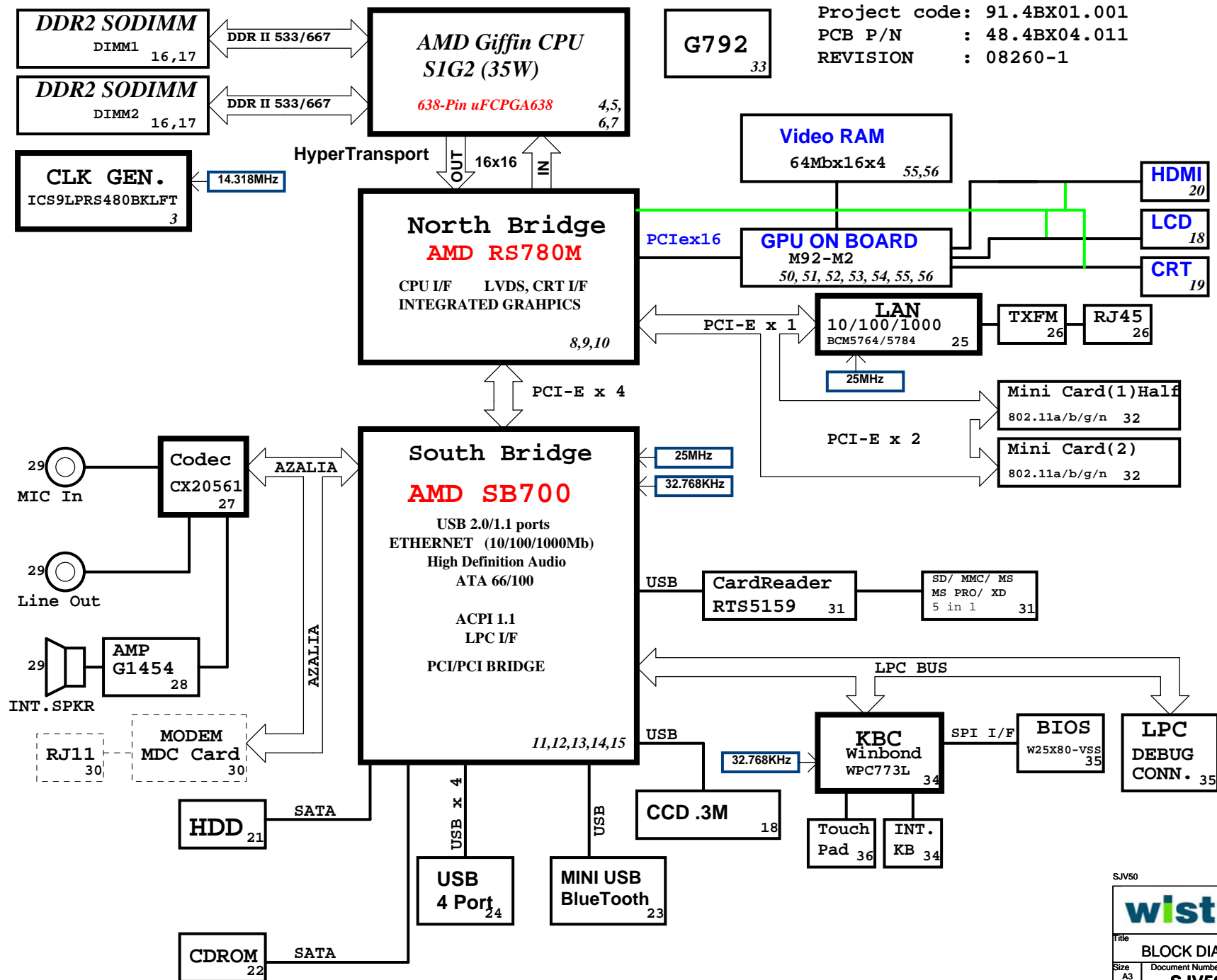


# SJV50-PU Block Diagram



SJV50

**wistron**

Wistron Incorporated  
 21F, 88, Hsin Tai Wu Rd  
 Hsichih, Taipei

File  
**BLOCK DIAGRAM**

Size A3  
 Document Number  
**SJV50-PU**

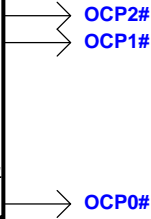
Date: Wednesday, February 25, 2009 Sheet 1 of 59

Rev  
 -1

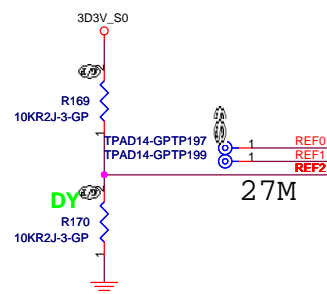
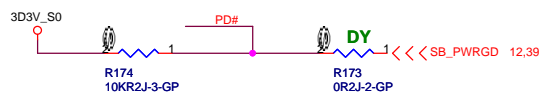
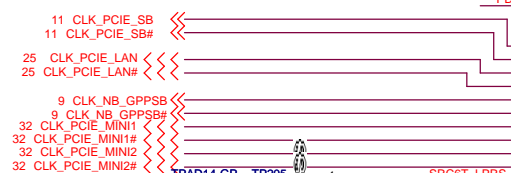
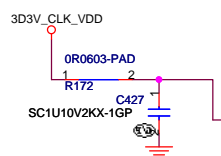
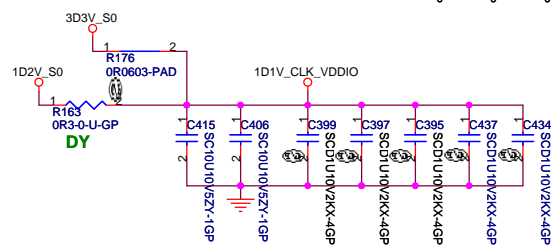
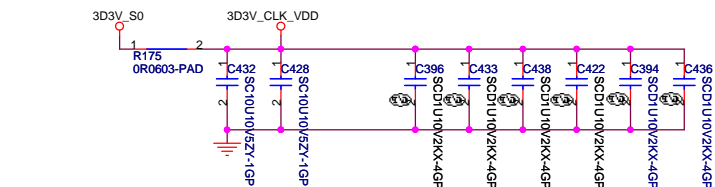
PCIE

PCIE0	LAN
PCIE1	MINICARD1
PCIE2	MINICARD2
PCIE3	

USB	
Pair	Device
11	CardReader
10	CCD
9	Mini Card2
8	USB4
7	USB1
6	USB2
5	BlueTooth
4	NC
3	NC
2	NC
1	Mini Card1
0	USB3

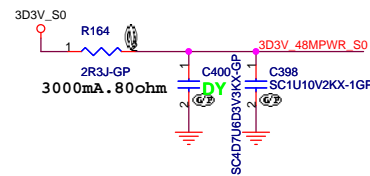


SJV50

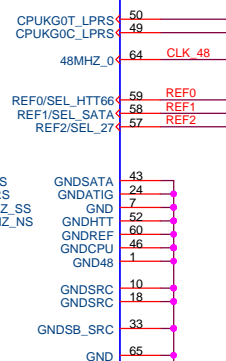
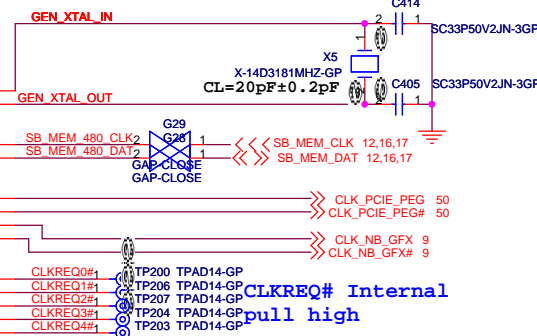


SEL_SATA REF1	1	100 MHz non-spreading differential SRC clock
	0*	100 MHz spreading differential SRC clock
SEL_HTT66 REF0	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_27 REF2	1*	27 MHz 3.3V single ended enable
	0	100 MHz spreading differential SRC clock

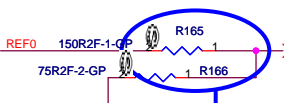
\* default  
CPU\_CLK (200MHz)



82.30005.A11  
2ND = 82.30005.881



20090107\_SB modify



OSC 14M NB  
RS780M 1.1V 158R/90.9R

Due to PLL issue on current clock chip, the SBLink clock need to come from SRC clocks for RS740 and RS780. Future clock chip revision will fix this.

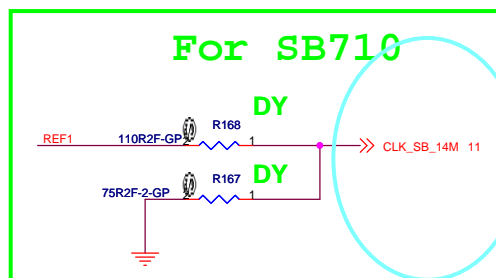
Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

\* RS780 can be used as clock buffer to output two PCIe reference clocks  
By default, chip will configured as input mode, BIOS can program it to output mode.

For SB710



SA\_20081106

SJV50

緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title Clock Generator ICS9LPRS480BKLT

Size Document Number

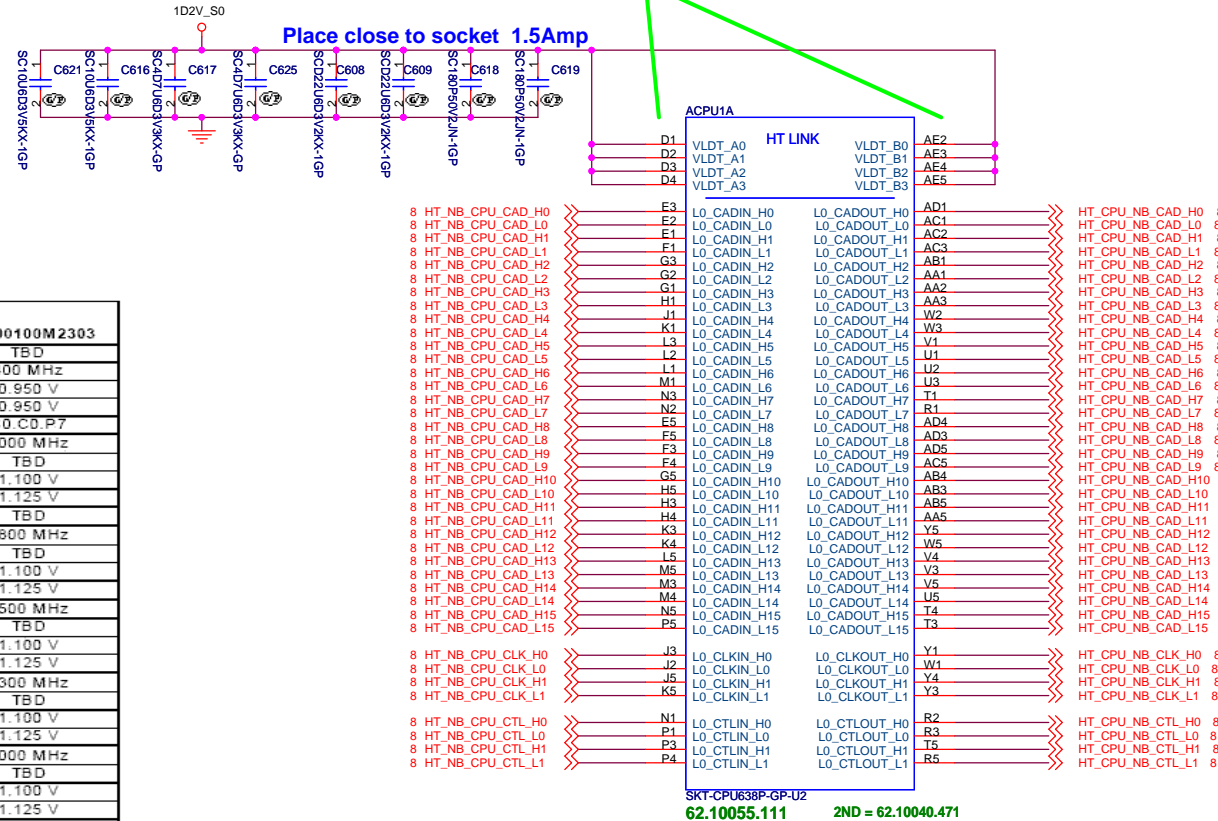
SJV50-PU

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Placement note:  
10ux1,4.7ux1,0.22ux1,180px1 for each group



SKT-BGA638H176

State	Specification	Notes	2M200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	1500 MHz
S0.C0.P2	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	1300 MHz
	TDP	3	TBD
S0.C0.P3	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
S0.C0.P4	VID_VDD Max	2	1.125 V
	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P5	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	300 MHz
S0.C0.P6	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	300 MHz
	TDP	3	TBD
S0.C0.P7	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V

SJV50

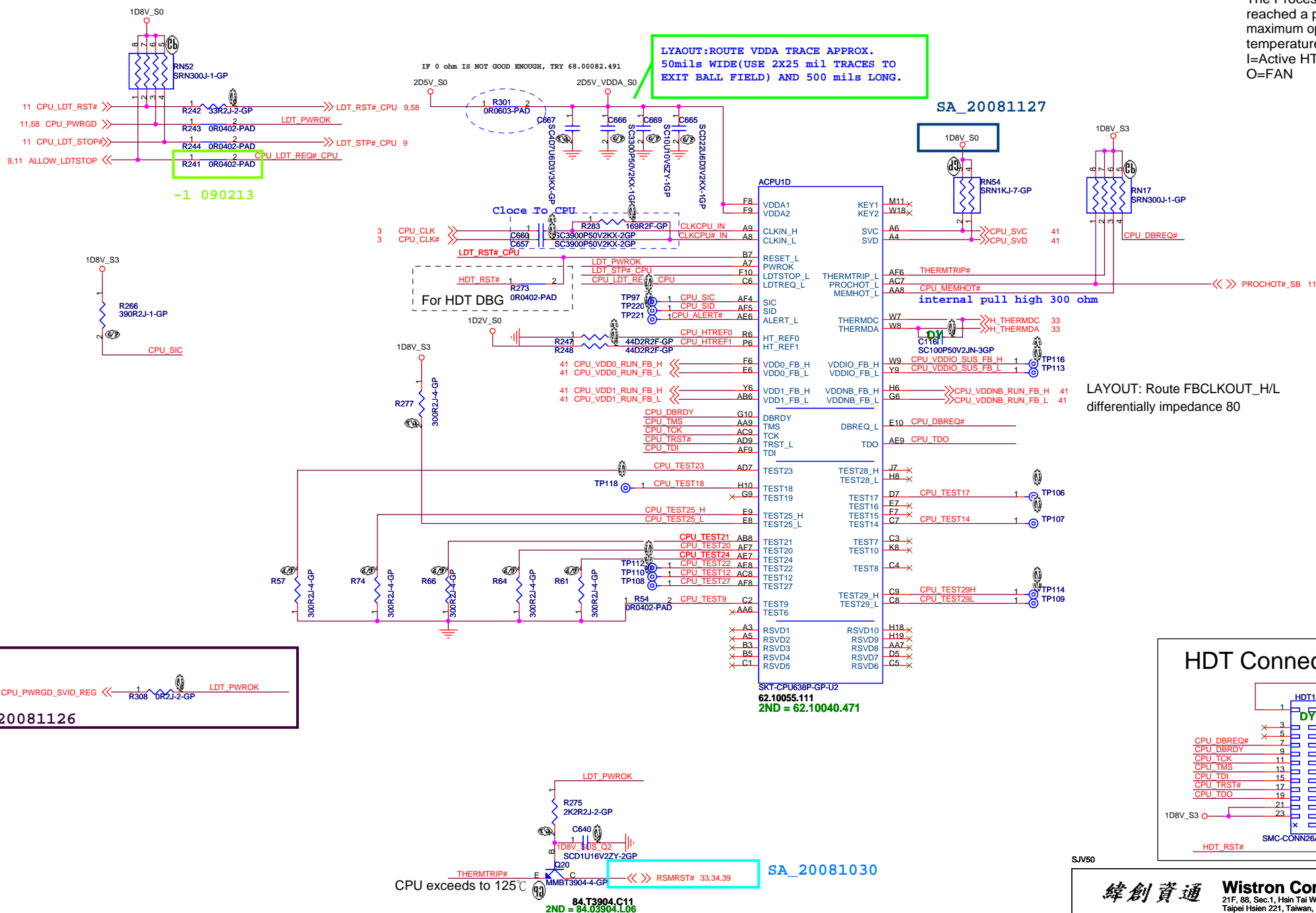
緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,  
Taipei Hsien 221, Taiwan, R.O.C.



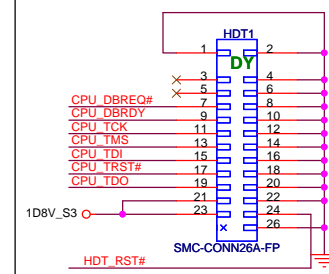
SKT-CPU638P-GP-U2  
**62.10055.111**

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The Processor has reached a preset maximum operating temperature. 100°C  
I=Active HTC  
O=FAN



## HDT Connectors

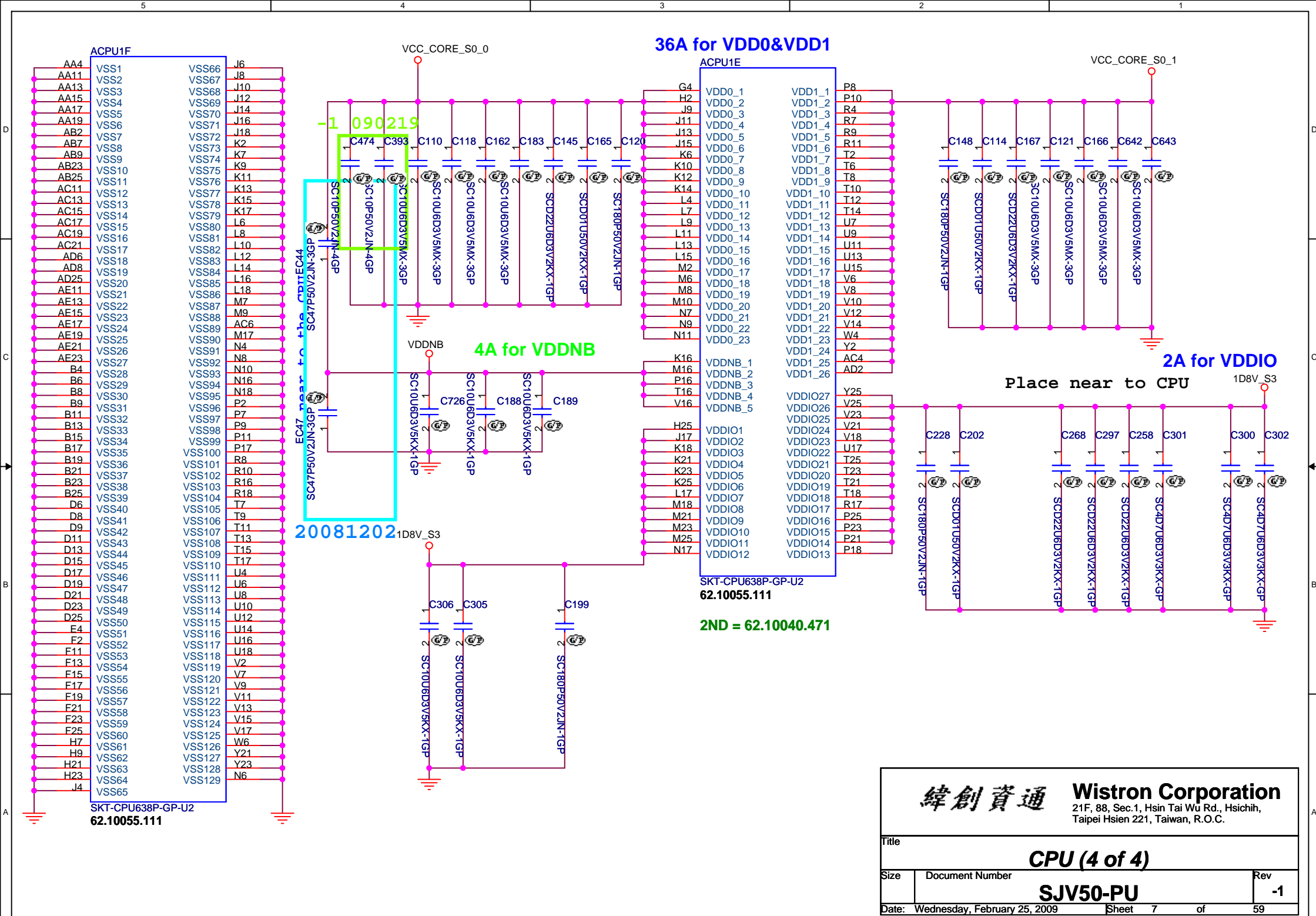


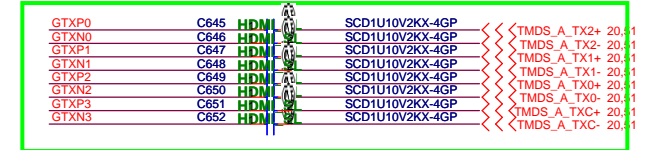
SJV50

**緯創資通** **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			
<b>CPU (3 of 4)</b>			
Size	Document Number	Rev	
	<b>SJV50-PU</b>	-	
Date:	Wednesday, February 25, 2009	Sheet	6 of 59



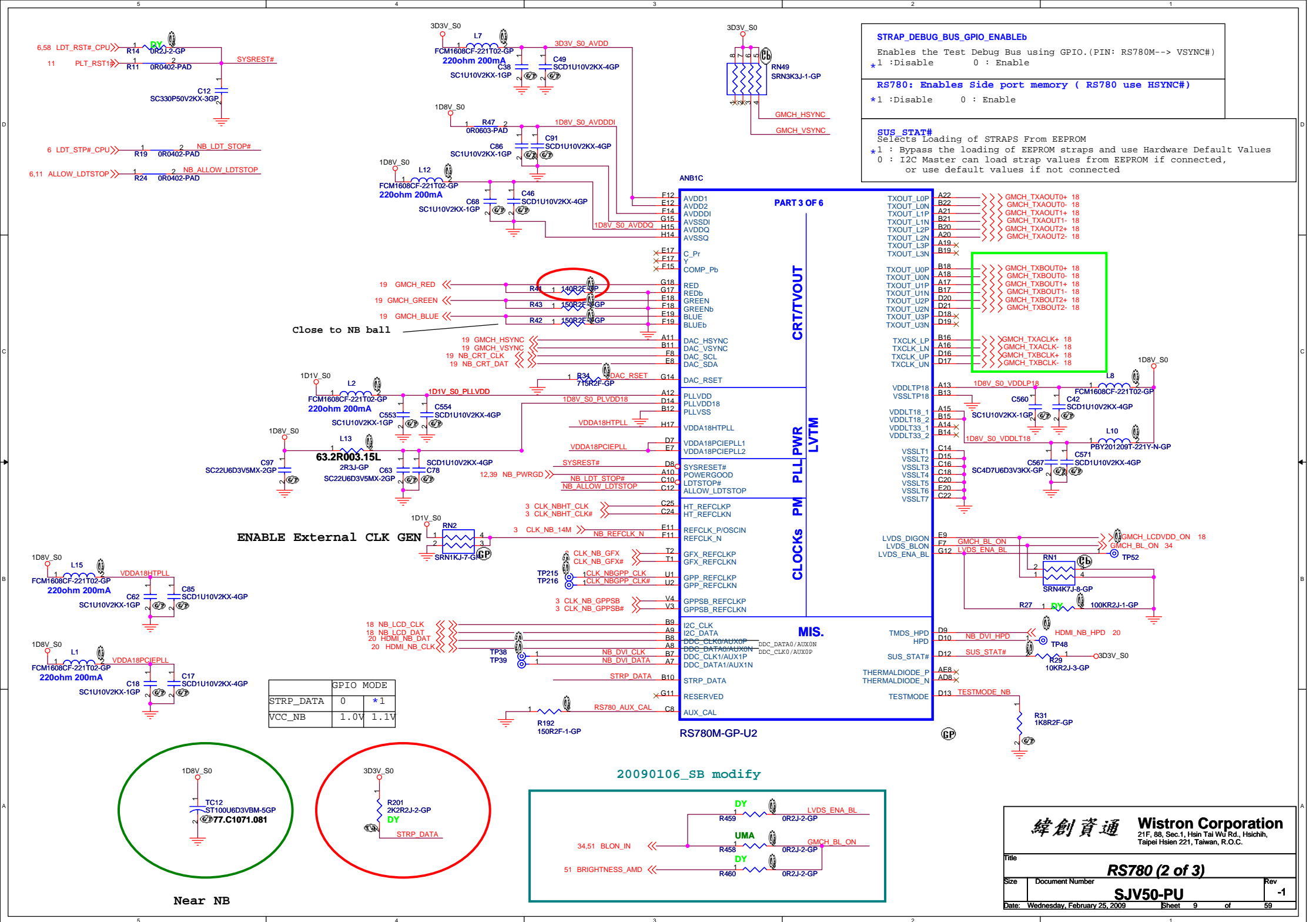




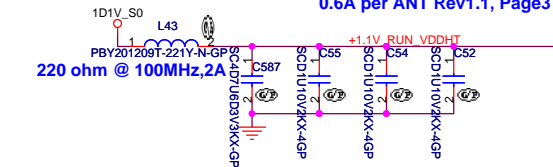
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DP1	GFX_TX4, TX5, TX6, TX7, AUX1, HPD1



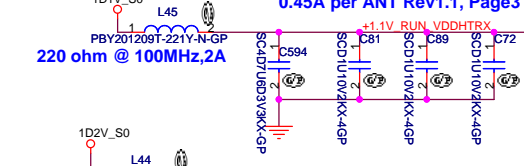




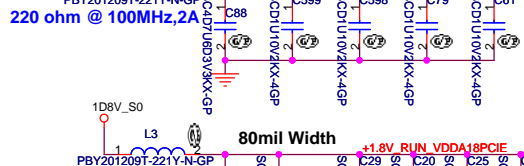
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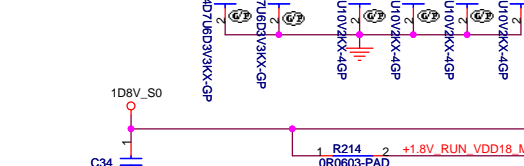
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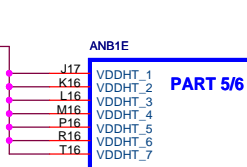
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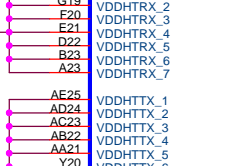
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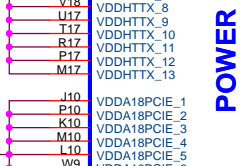
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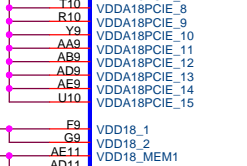
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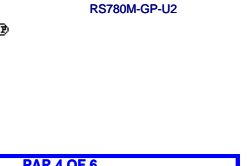
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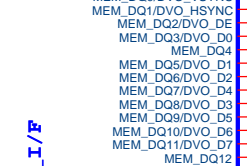
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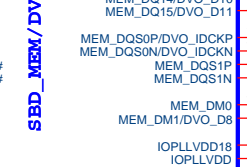
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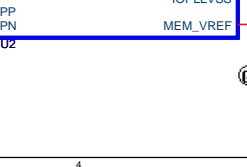
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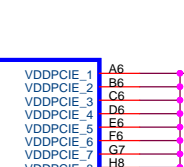
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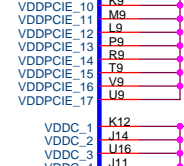
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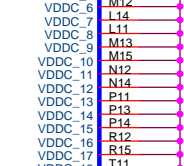
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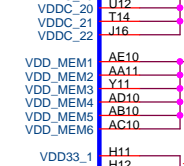
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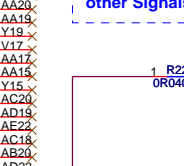
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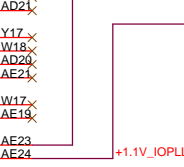
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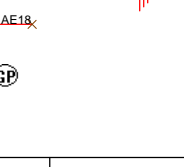
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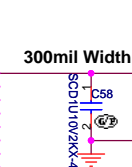
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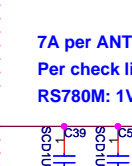
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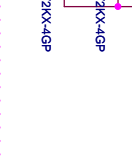
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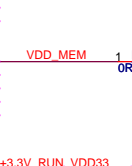
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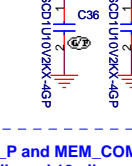
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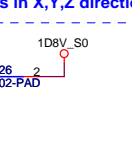
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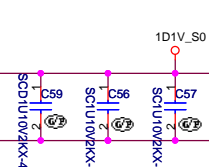
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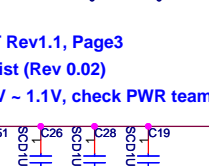
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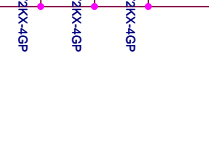
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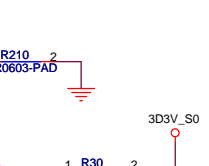
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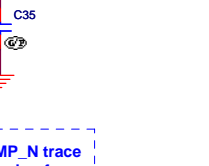
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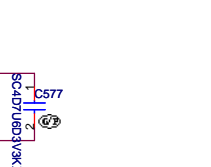
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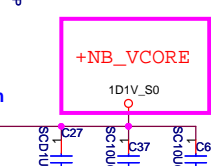
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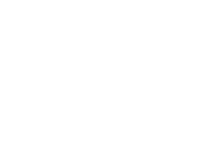
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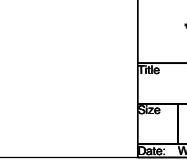
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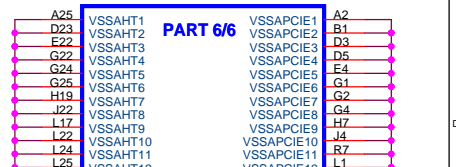
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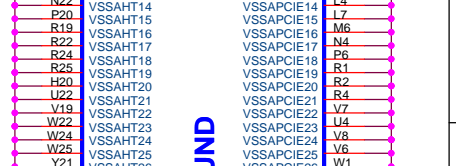
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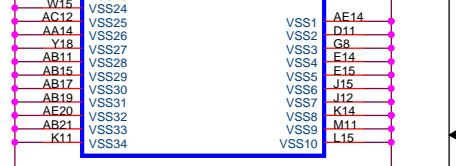
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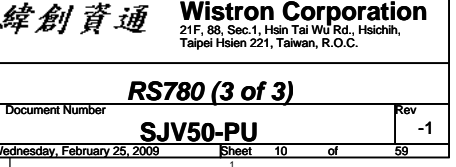
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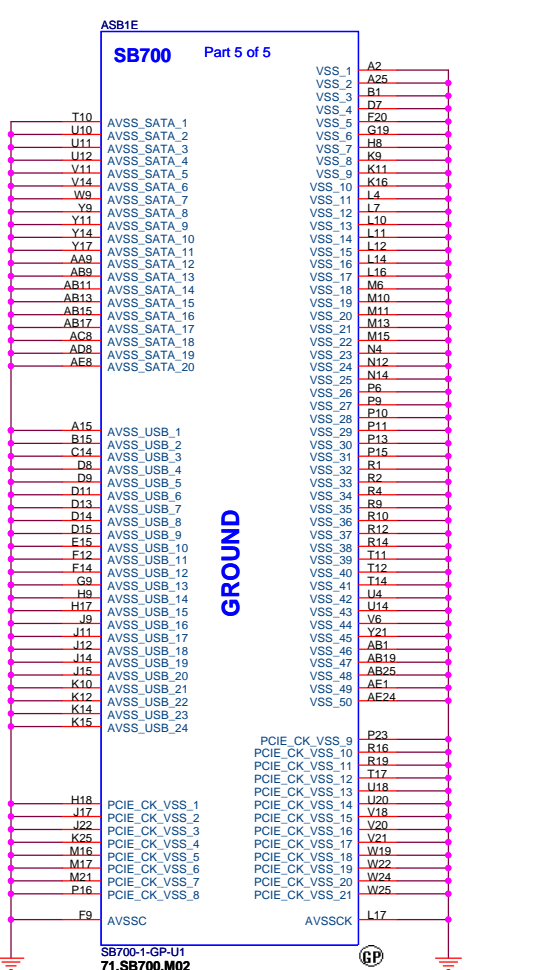
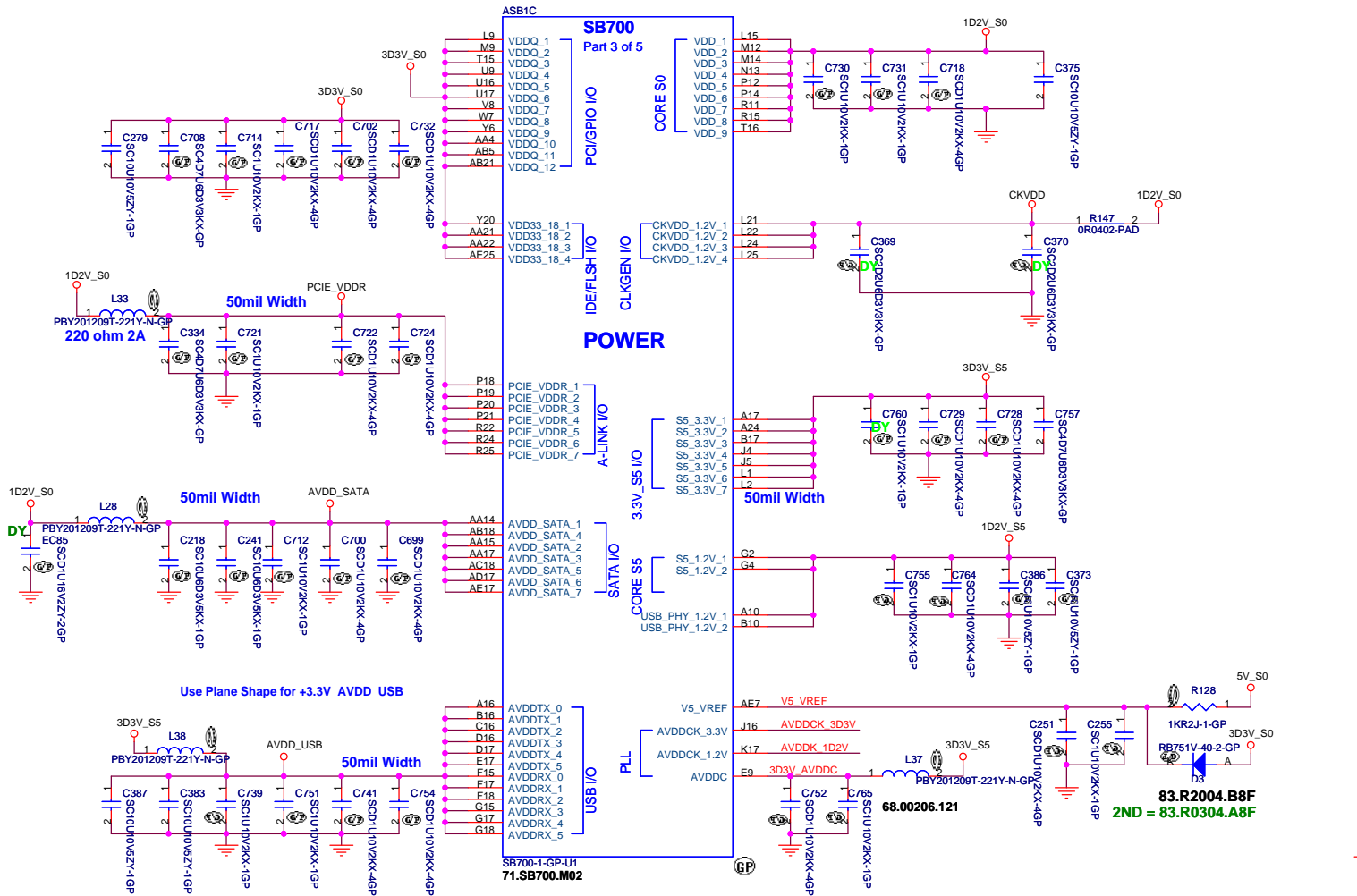


緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,  
Taipei Hsien 22







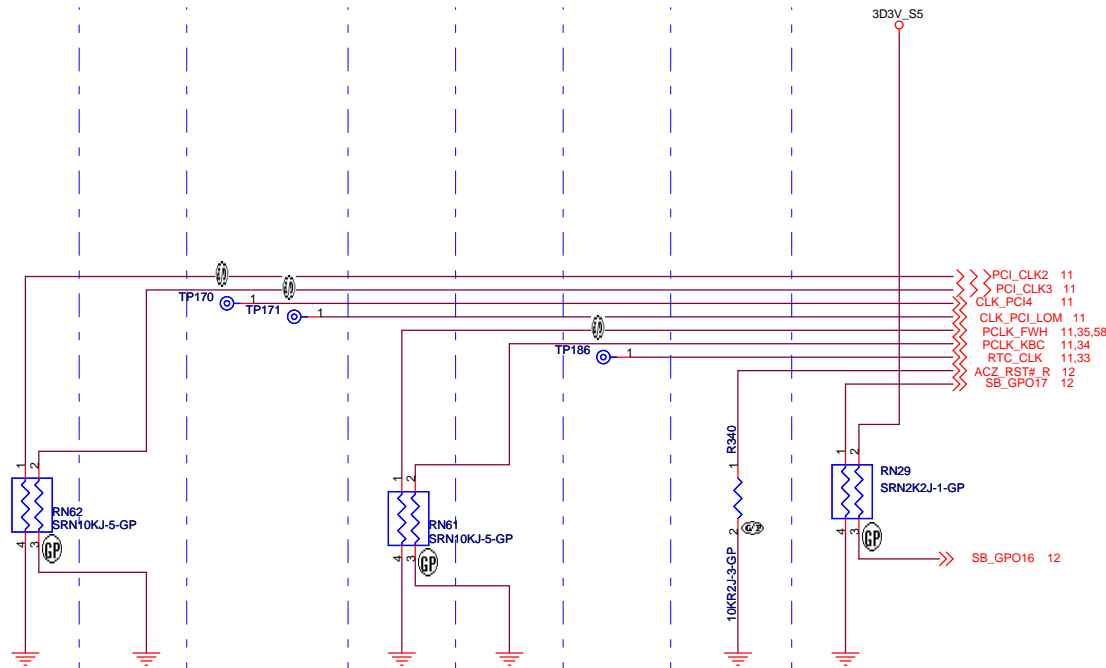




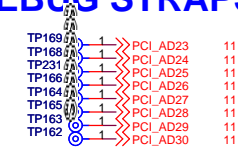
## Delete DY Parts

## REQUIRED STRAPS

### REQUIRED SYSTEM STRAPS



## DEBUG STRAPS



	PCI_CLK2	PCI_CLK3	CLK_PCI_LOM CLK_PCI4	PCLK_FWH	PCLK_KBC	RTCCLK	AZ_RST#	SB_GPO17, SB_GPO16
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	IMC ENABLED	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT	ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		IMC DISABLED DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT	L, H = LPC ROM L, L = FWH ROM

**NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK**

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	

Note: SB700 has 15K internal PU FOR PCI\_AD[30:23]

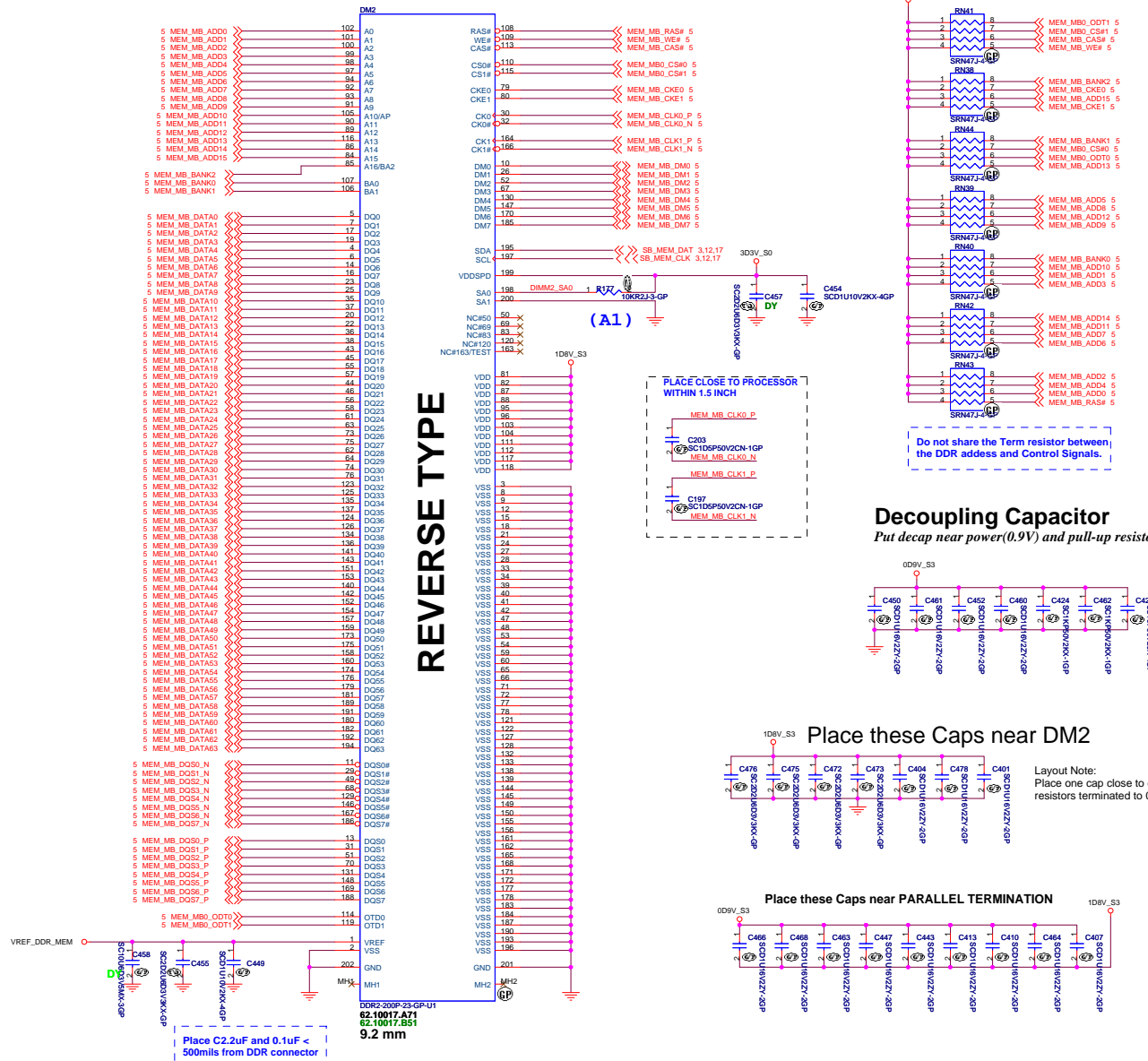
緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			<b>SB700 (5 of 5)</b>		
Size	Document Number				Rev
	<b>SJV50-PU</b>				<b>-1</b>
Date:	Wednesday, February 25, 2009				Sheet 15 of 59

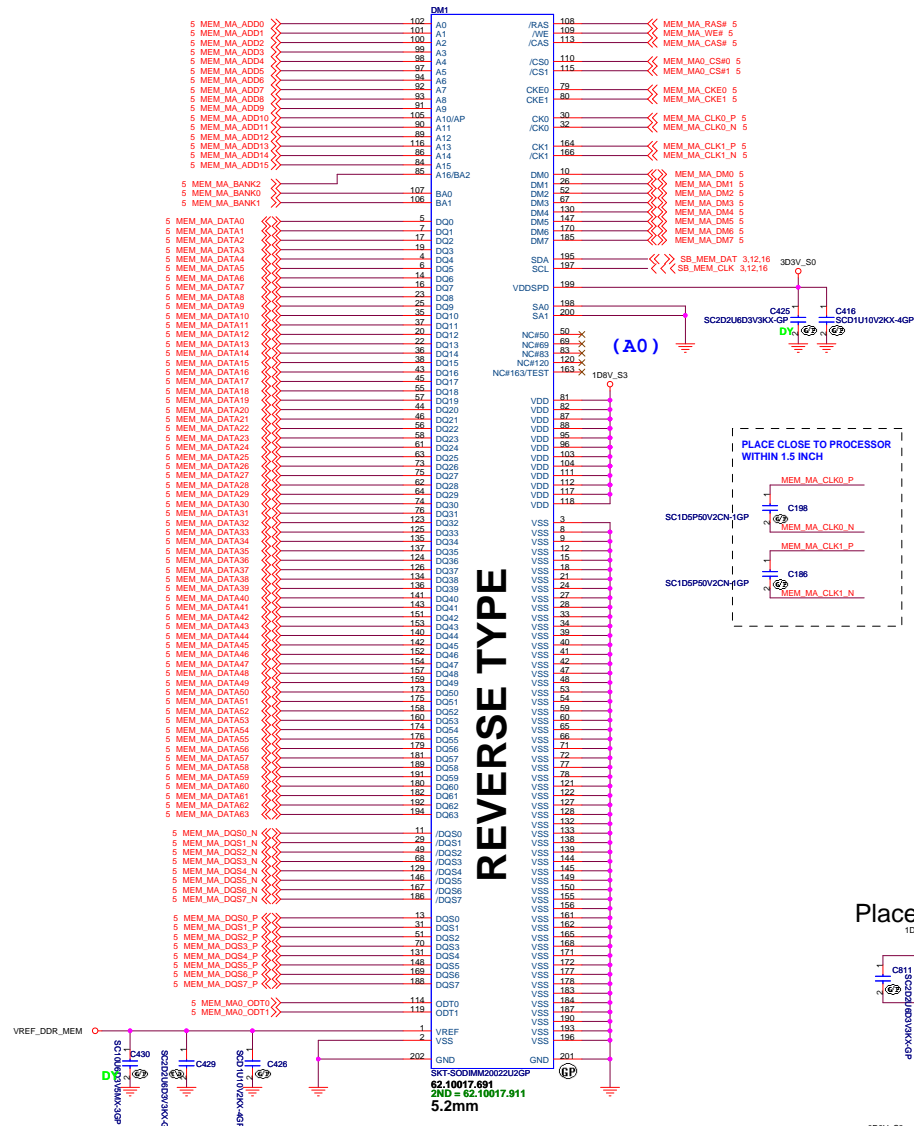
# DDR2 SOCKET\_2 (9.2mm)

## PARALLEL TERMINATION

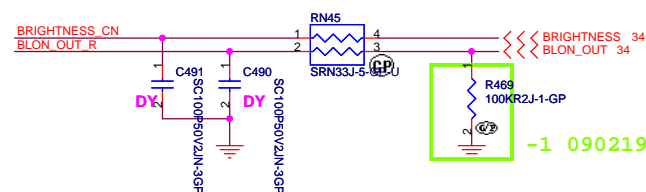
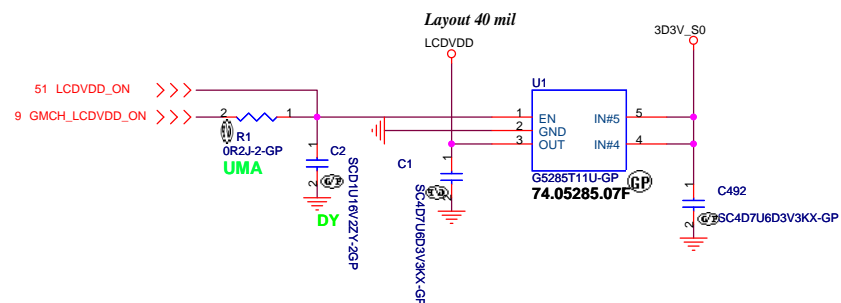
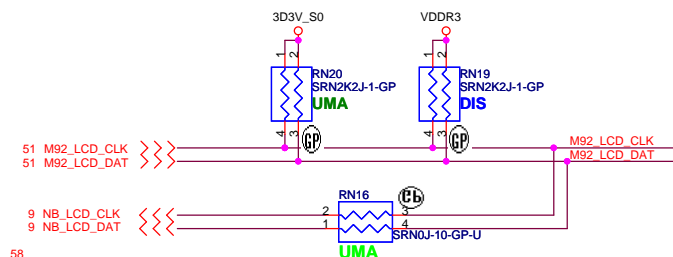
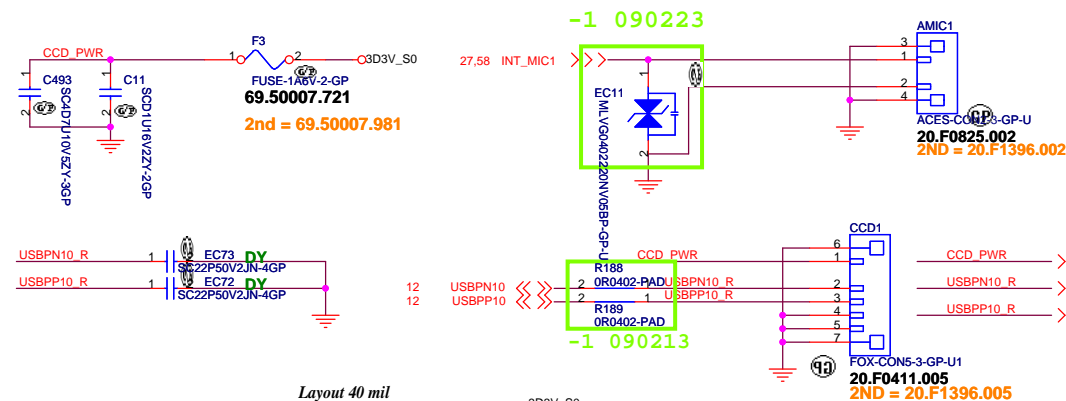
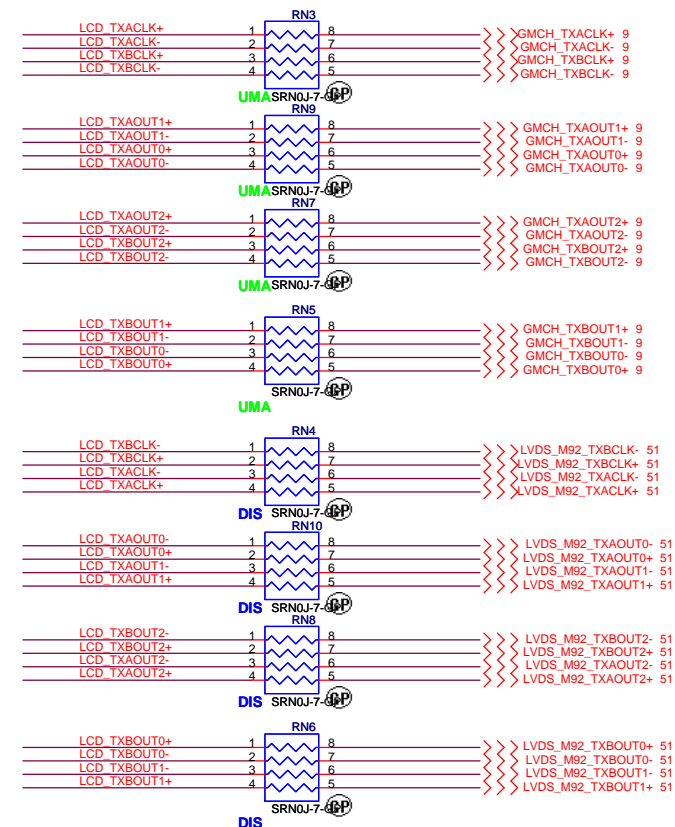
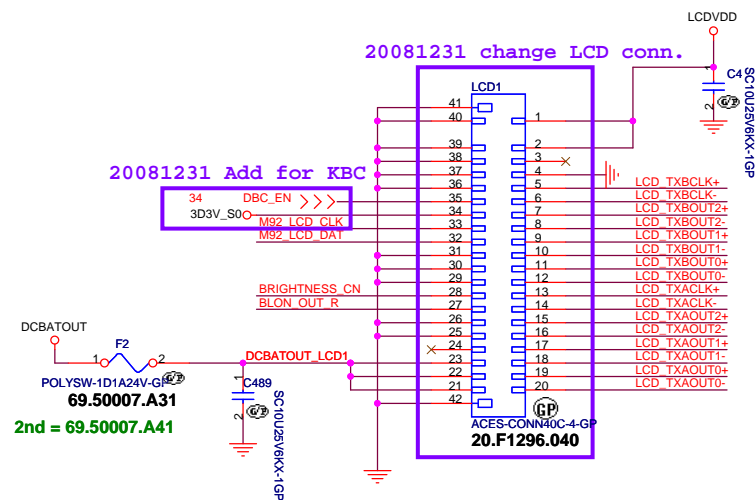
Put decap near power(0.9V) and pull-up resistor



# DDR2 SOCKET\_1 (5.2mm)



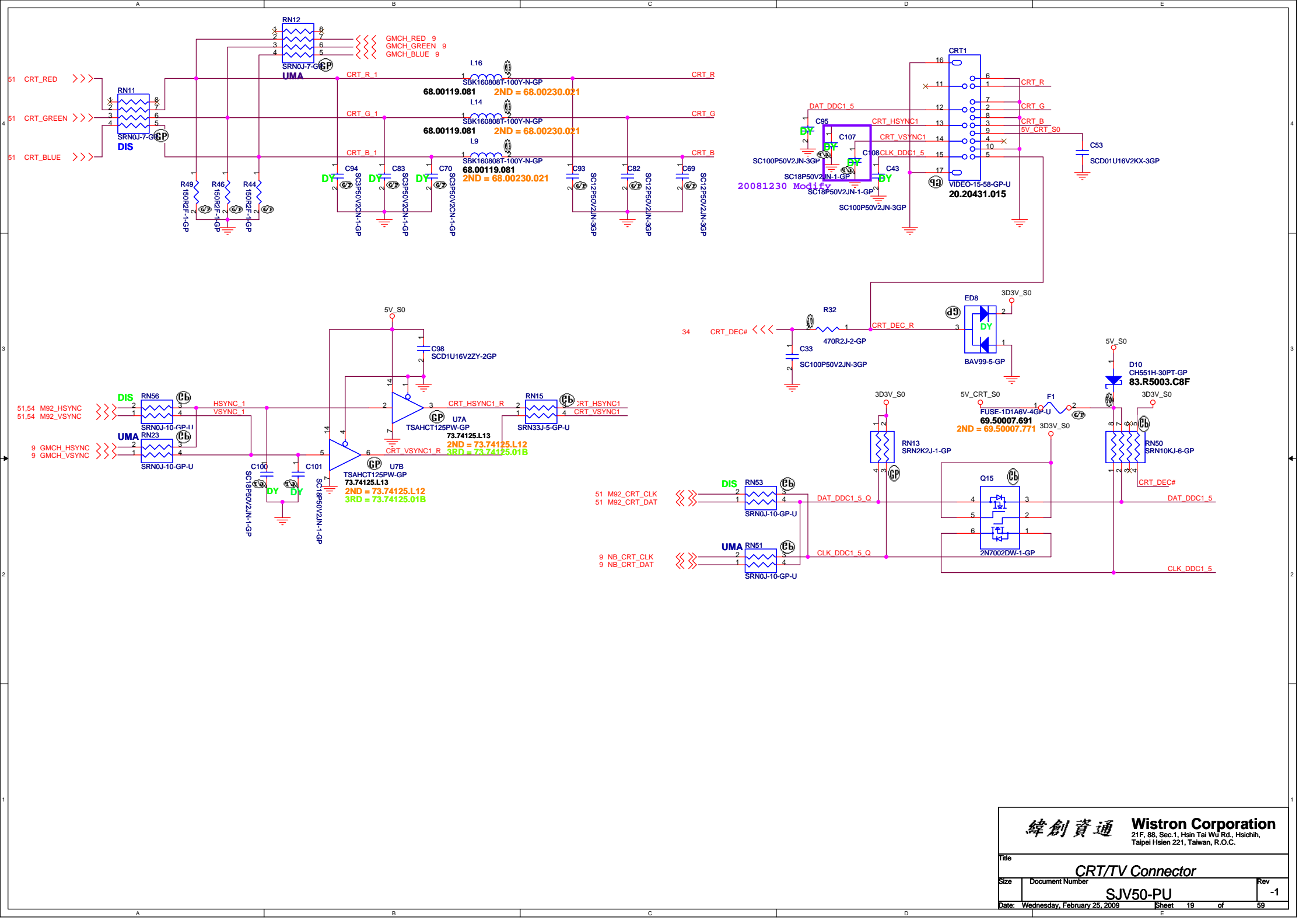
# LCD/CCD CONN

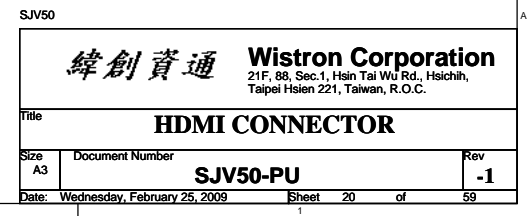


SJV50

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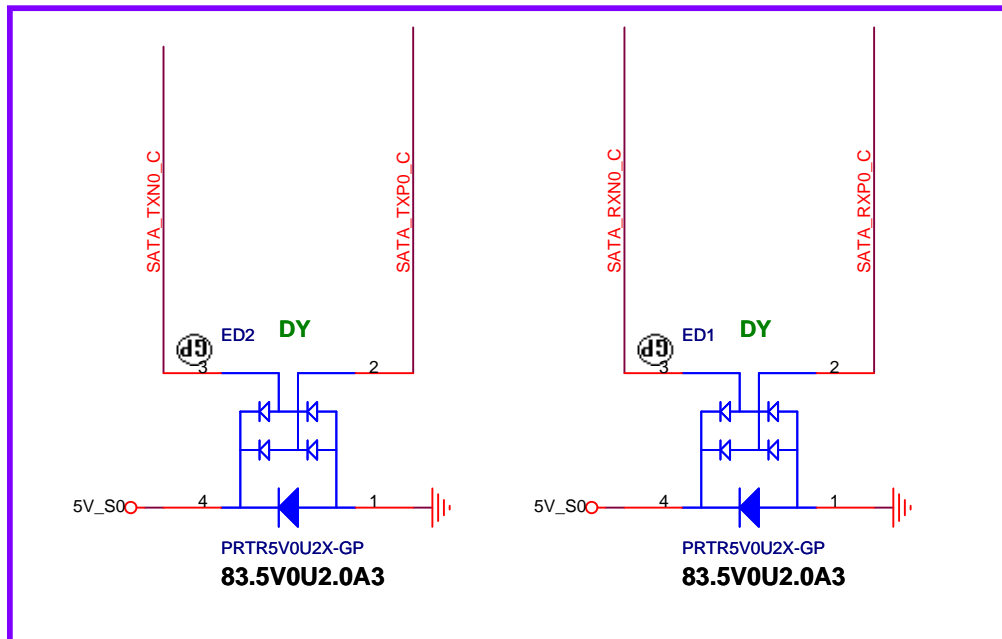
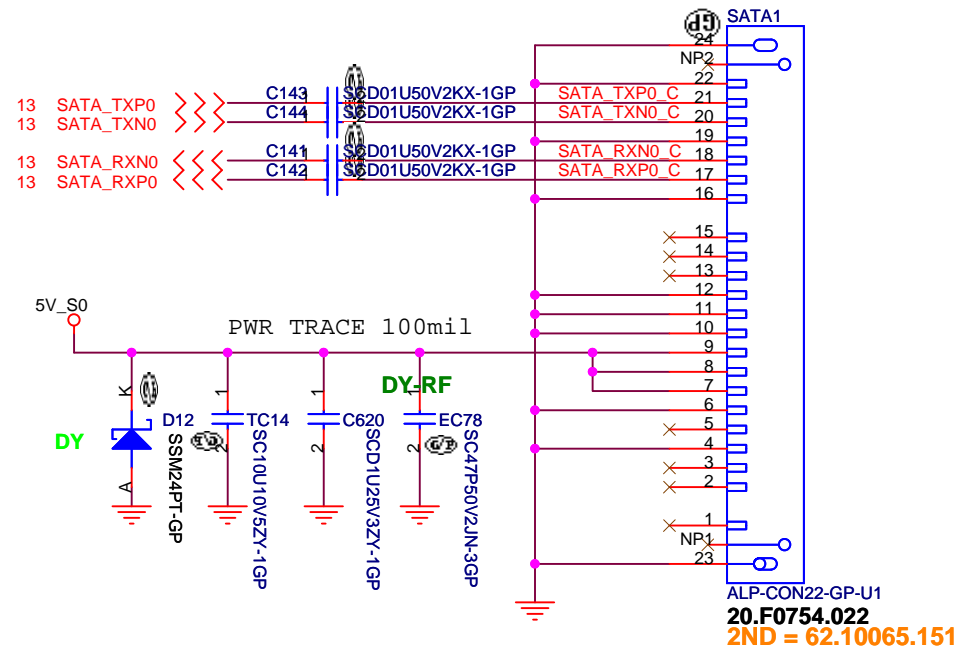
LED & LCD CONN / CCD			
Title	Document Number	SJV50-PU	
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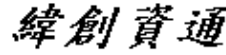


# SATA HDD Connector

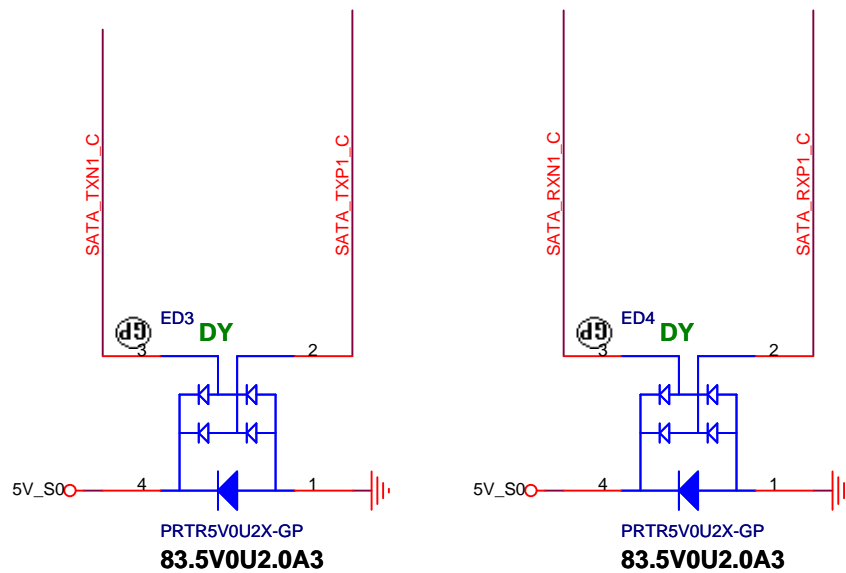
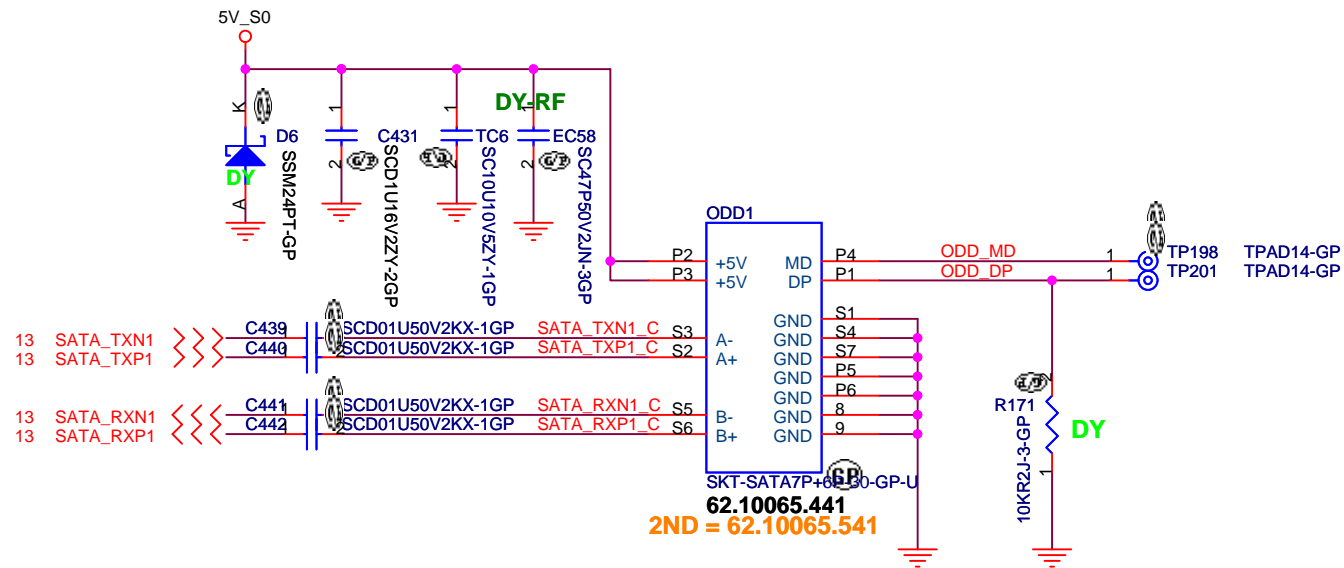


SA\_20081112

SJV50

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Title	
HDD	
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## SATA ODD Connector



**SJV50**

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Title
-------

***ODD***

Size

Document Number
-----------------

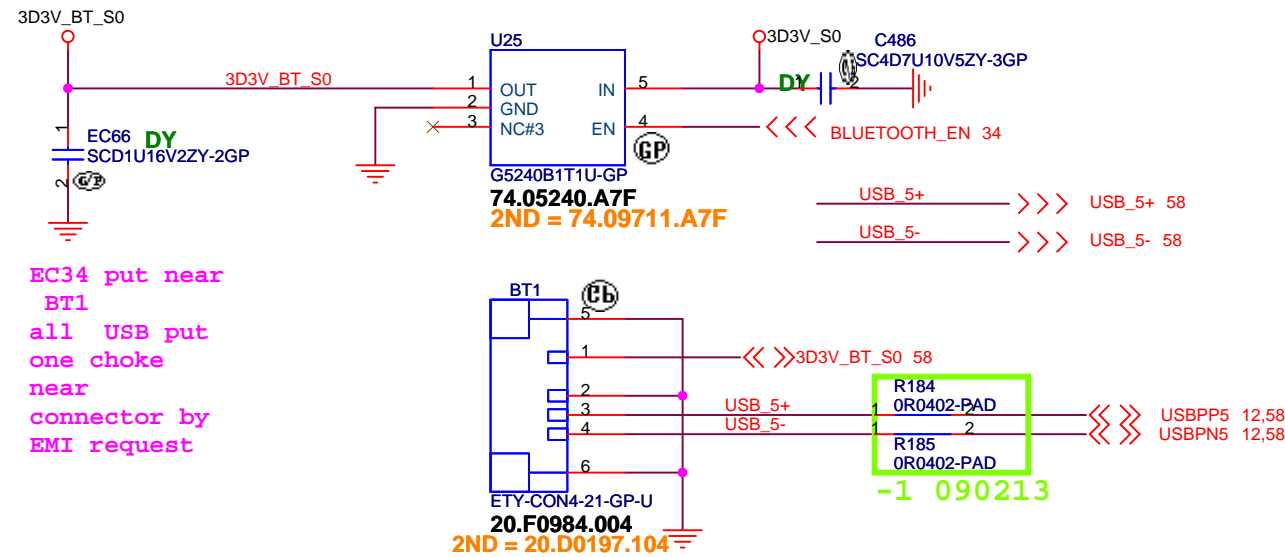
## **SJV50-PU**

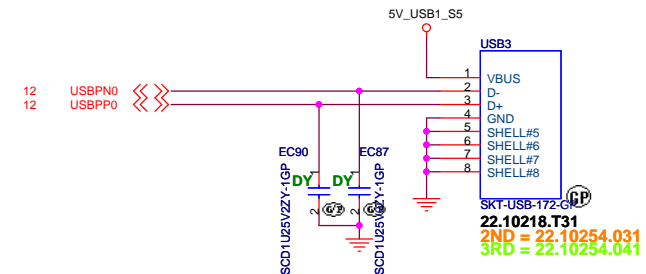
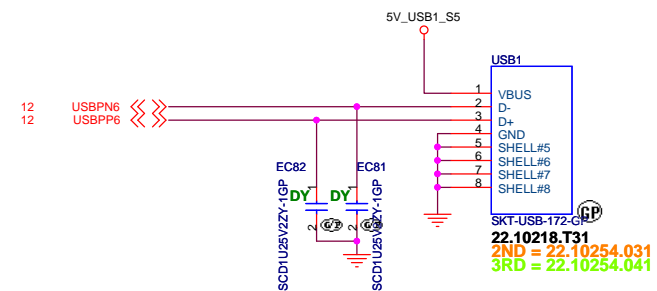
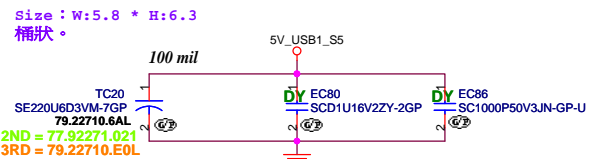
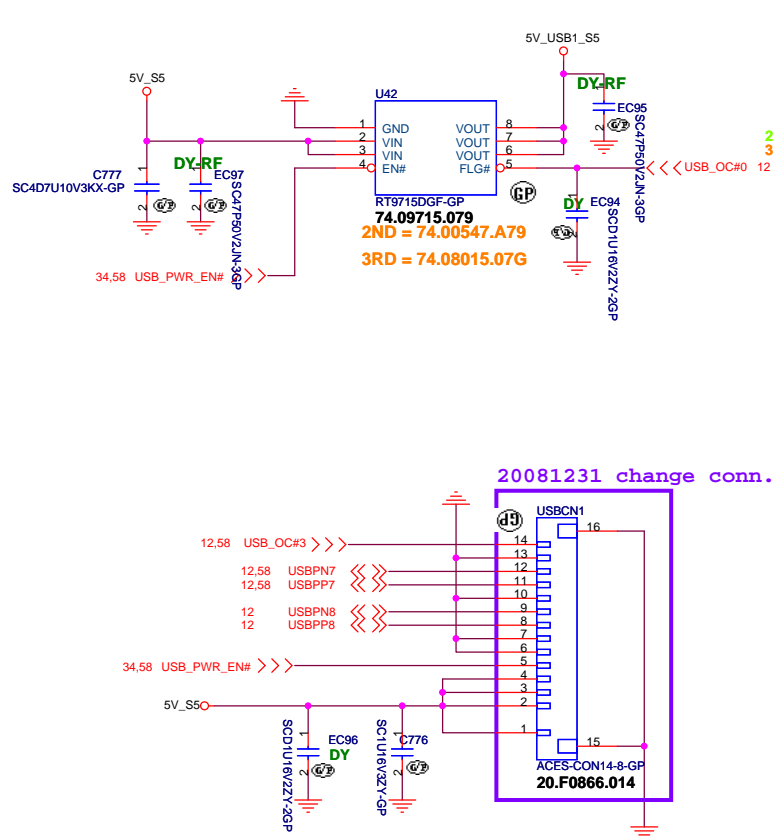
Rev  
-1

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BLUETOOTH MODULE

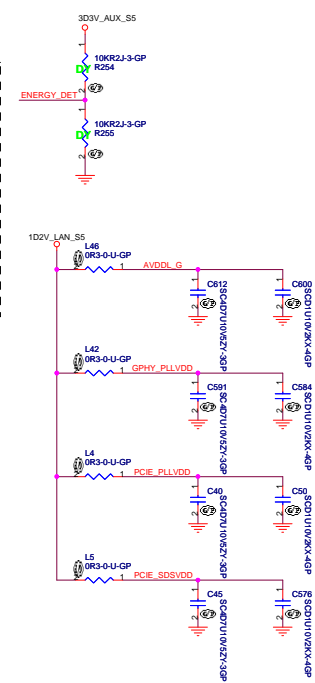




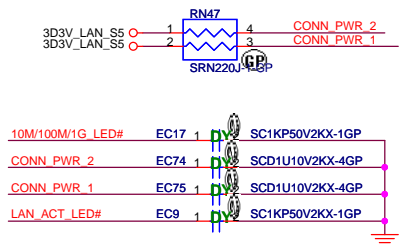
PD UMA

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Taipei Hsien 221, Taiwan, R.O.C.

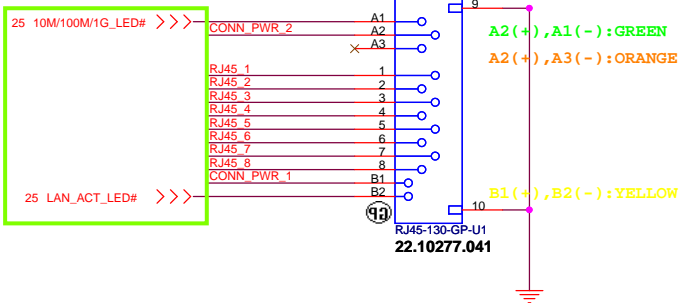
Title			
<b>USB Connector</b>			
Size	Document Number		Rev
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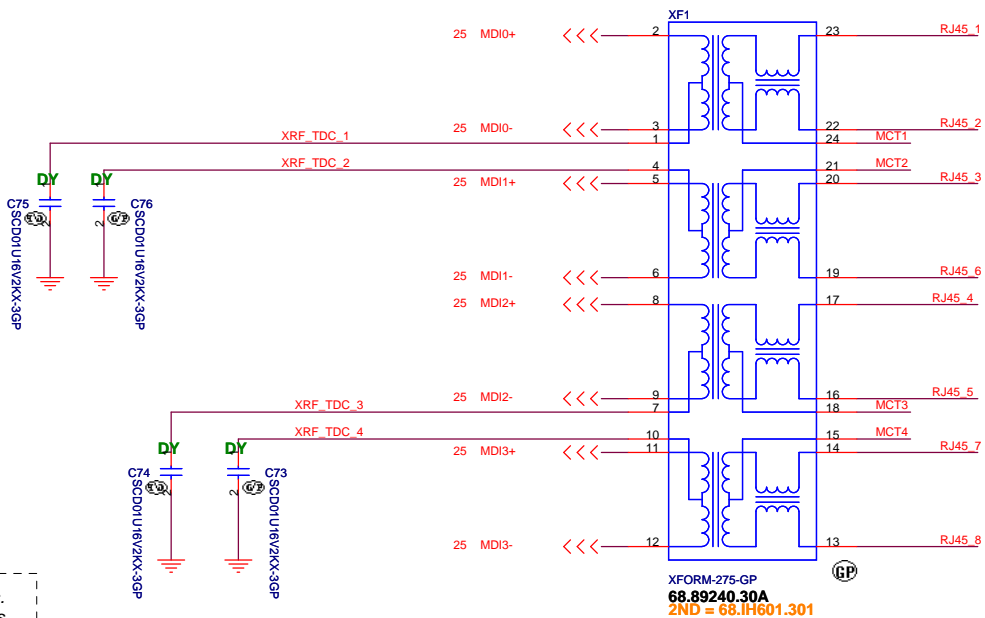
# LAN Connector



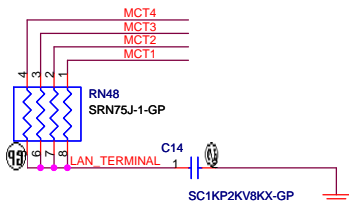
-1 090217



## GIGA Lan Transformer



- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat, except RJ-45 moat.



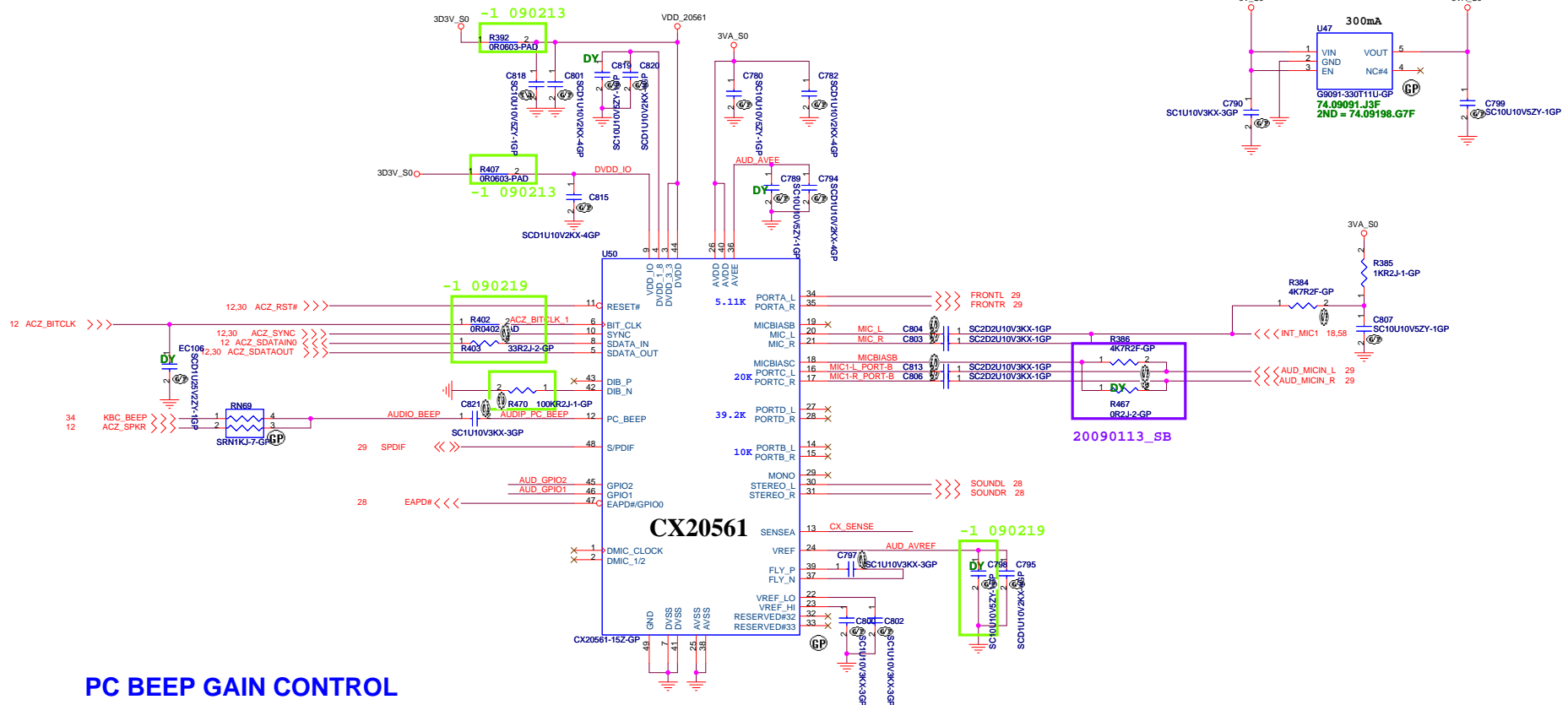
10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

SJV50

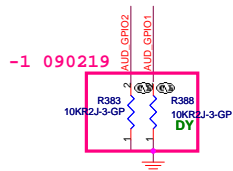
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Title LAN Connector  
Size A3 Document Number SJV50-PU Rev -1  
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## PC BEEP GAIN CONTROL



Default gain is -6dB without populating the 10K-ohms pull-down resistors going to GPIO1 and GPIO2.

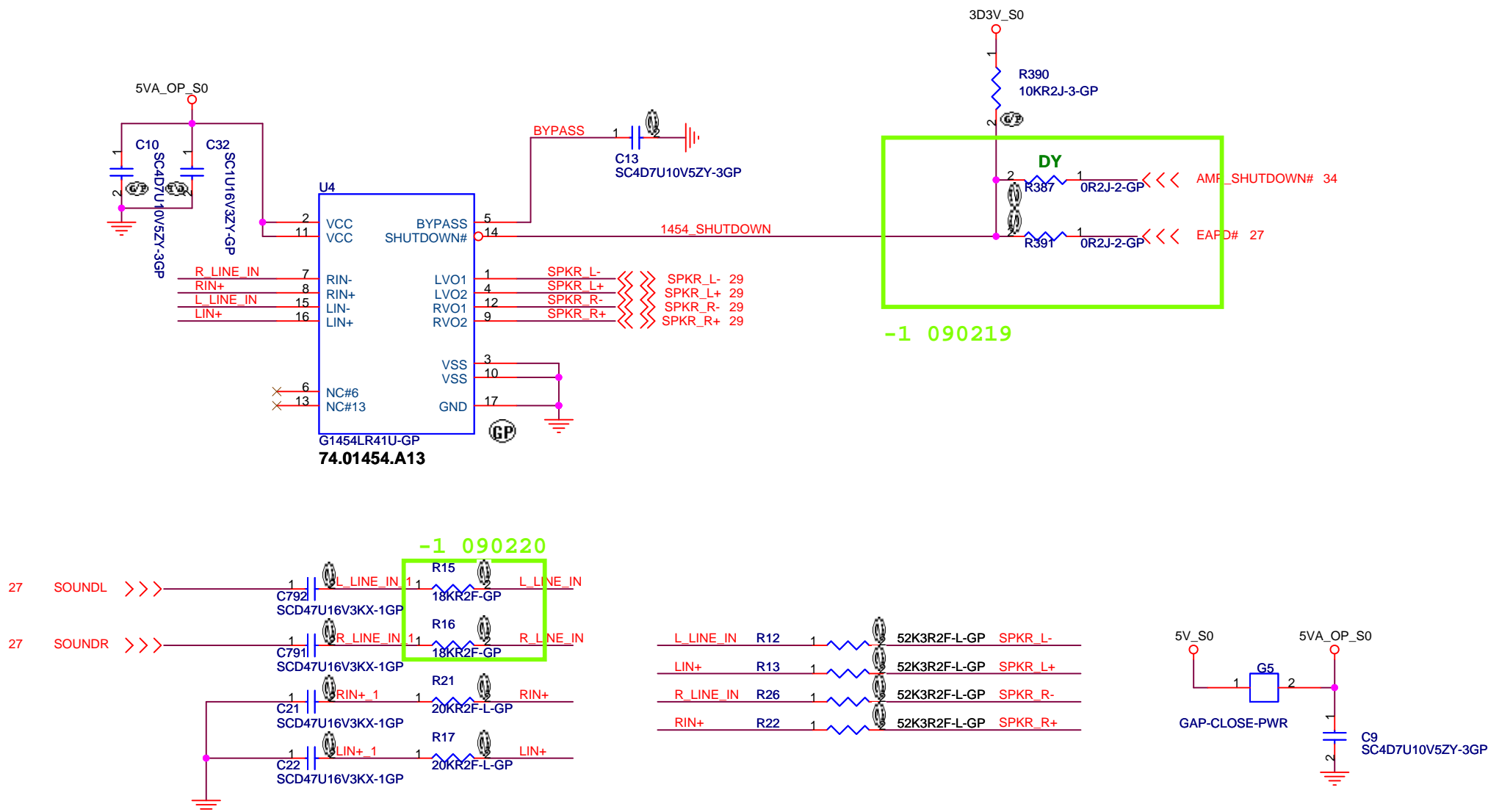
10K GPIO RESISTORS		
GAIN	R388	R389
0dB	Populate	Populate
-6dB	Omit	Omit
-12dB	Populate	Omit
-18dB	Omit	Populate

SJV50

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Title			AZALIA CODEC - CX20561
Size	Document Number	SJV50-PU	
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# AUDIO OP AMPLIFIER

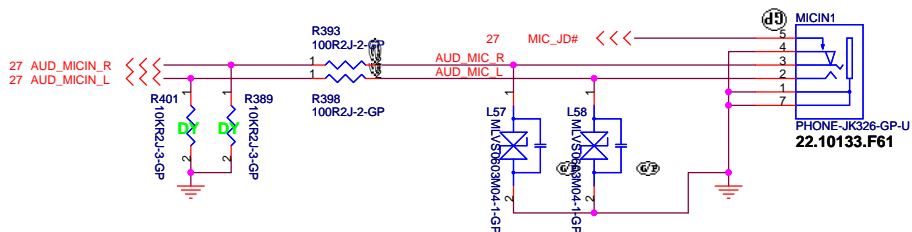


PD UMA

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Taipei Hsien 221, Taiwan, R.O.C.

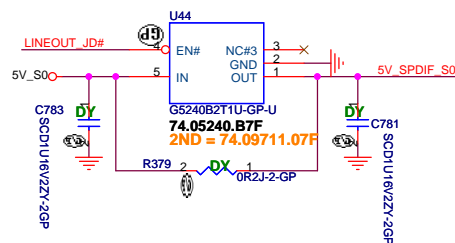
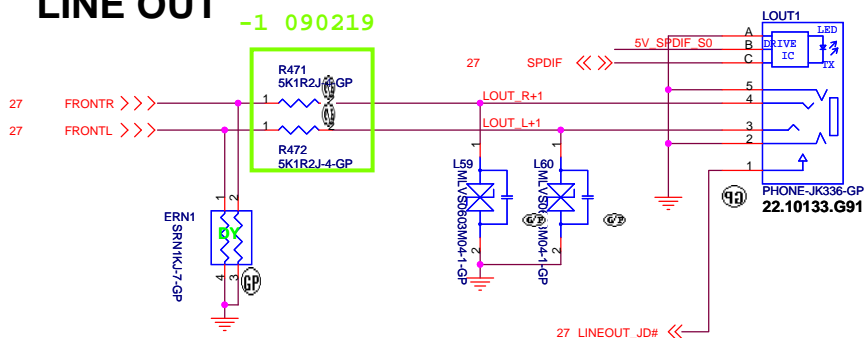
Title		
<b>AUDIO AMP (G1454)</b>		
Size	Document Number	Rev
	<b>SJV50-PU</b>	<b>-1</b>
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# MIC IN



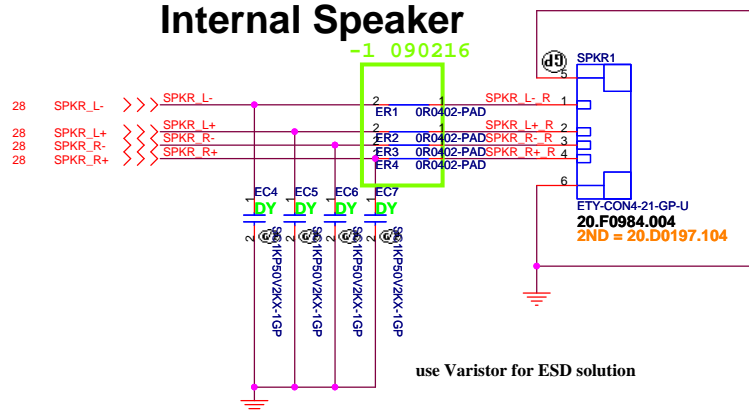
# LINE OUT

-1 090219



# Internal Speaker

-1 090216



use Varistor for ESD solution

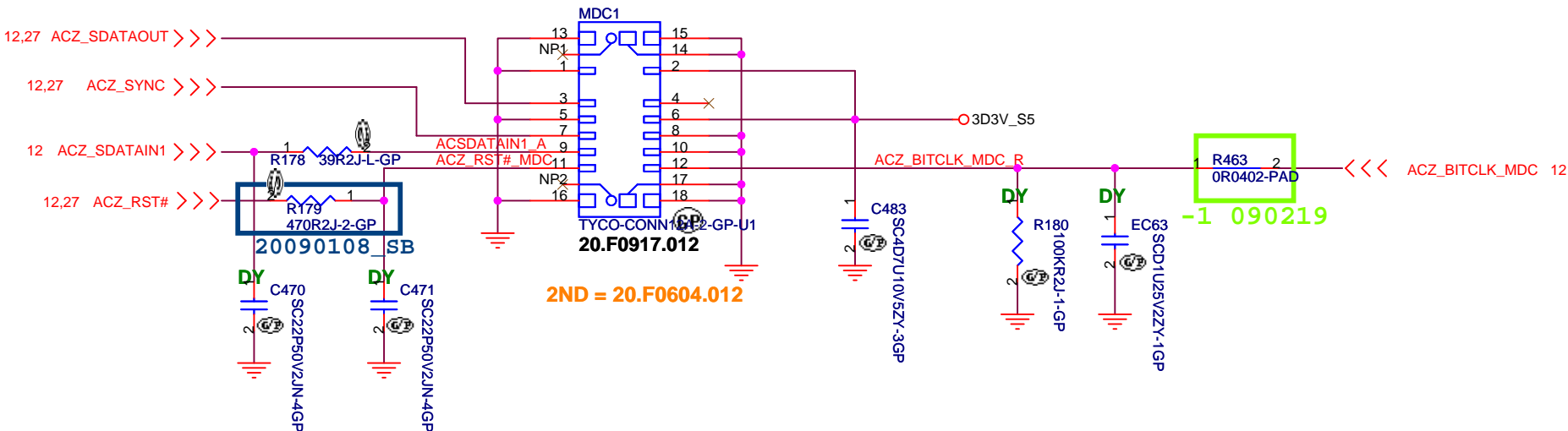
SPKR\_L- R 58  
SPKR\_L+ R 58  
SPKR\_R- R 58  
SPKR\_R+ R 58

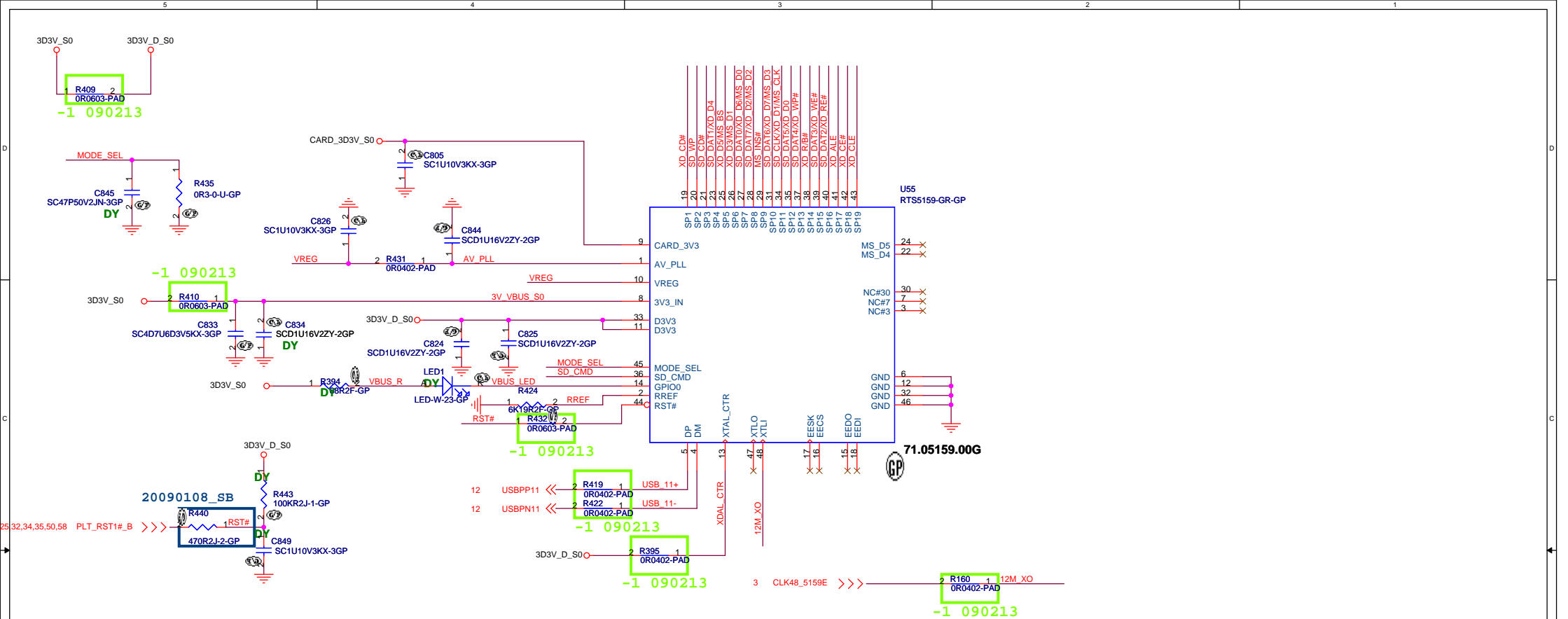
SJV50

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Taipei Hsien 221, Taiwan, R.O.C.

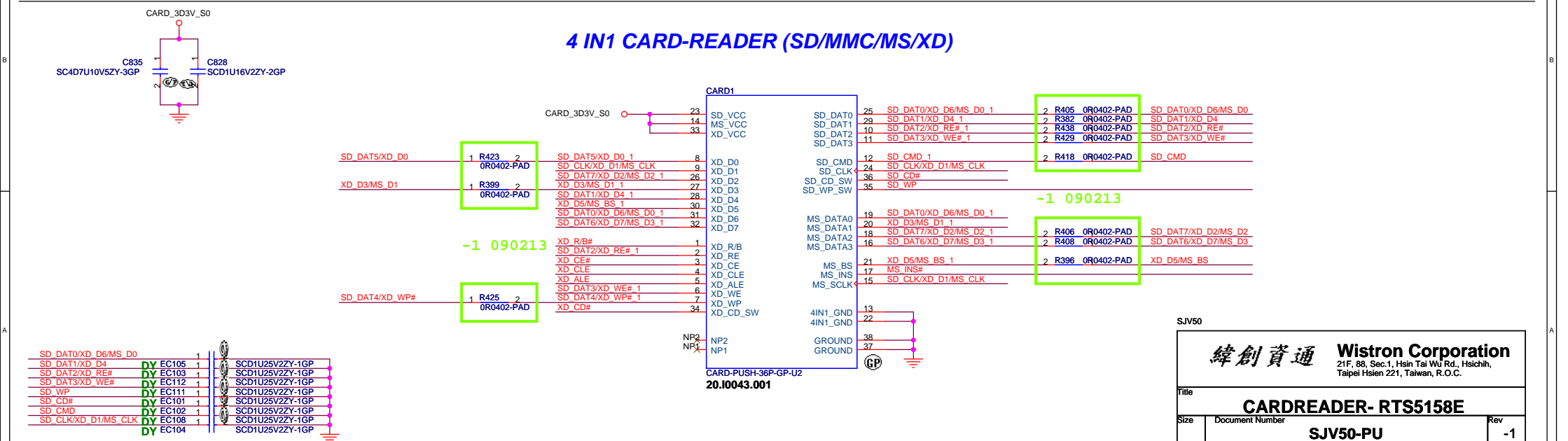
Title		
Audio Jack		
Size	Document Number	Rev
	SJV50-PU	-1
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MDC 1.5 CONN





## 4 IN1 CARD-READER (SD/MMC/MS/XD)

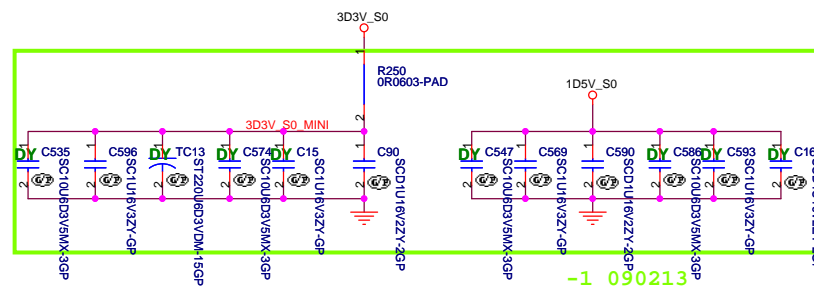
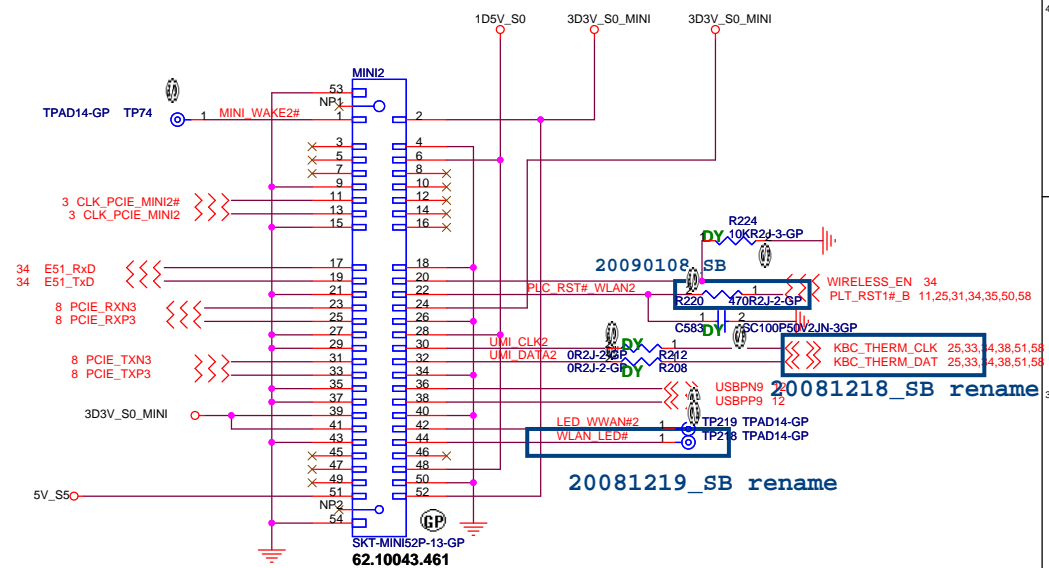
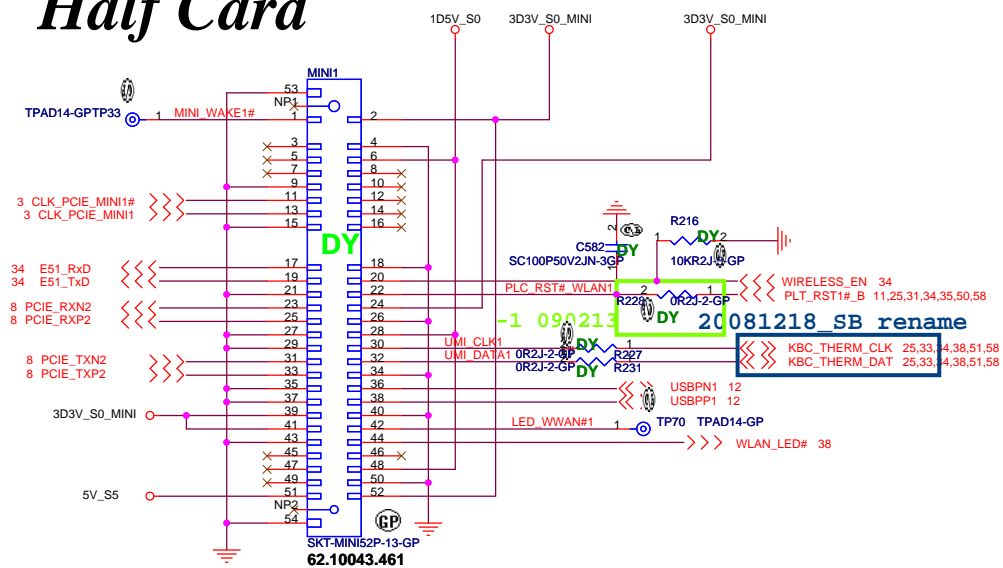


SJV50

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CARDREADER- RTS5158E		
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### *Half Card*



SJV50

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Title	Author	Date	Page	Page	Page	Page	Page	Page	Page	Page	Page
Title	Author	Date	Page	Page	Page	Page	Page	Page	Page	Page	

**MINI CARD**

Size

Document Number

Rev

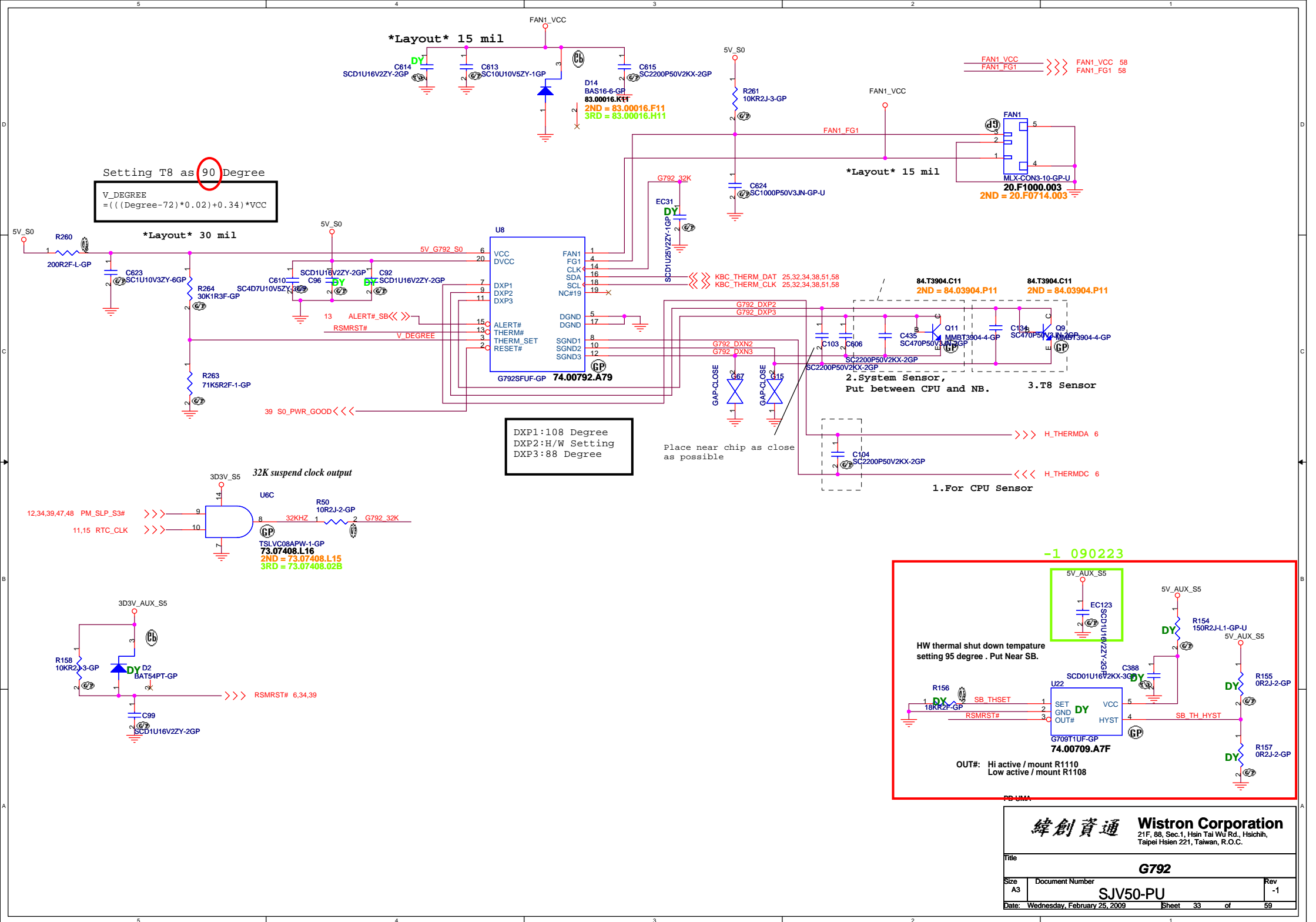
## **SJV50-PU**

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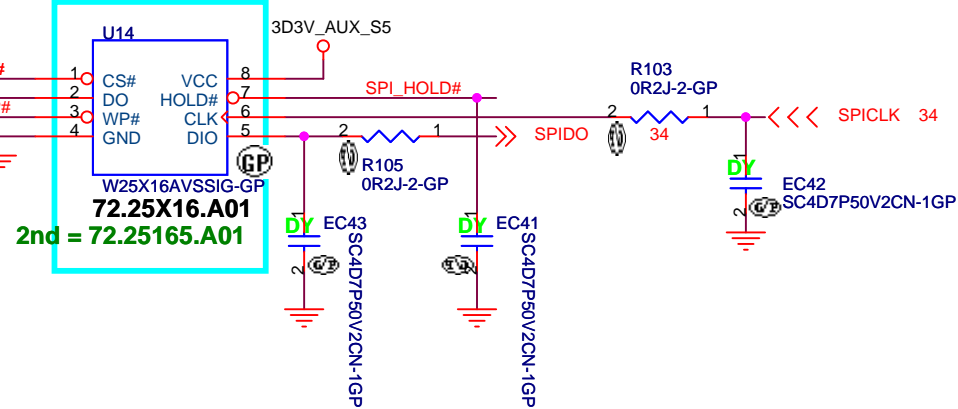




## SPI FLASH ROM

16M Bits

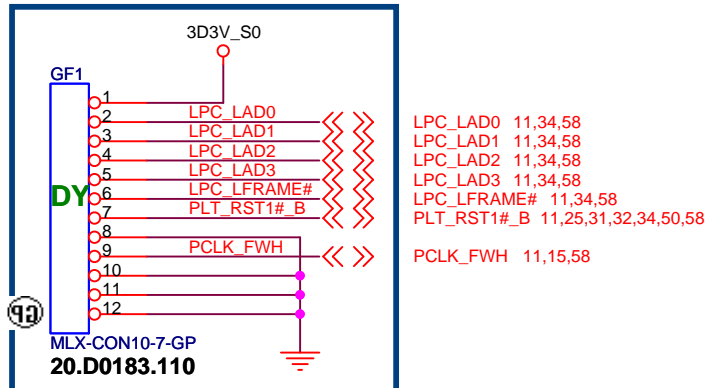
20081208



EMI REQUEST

## Connector FOR DEBUG BOARD

20081219

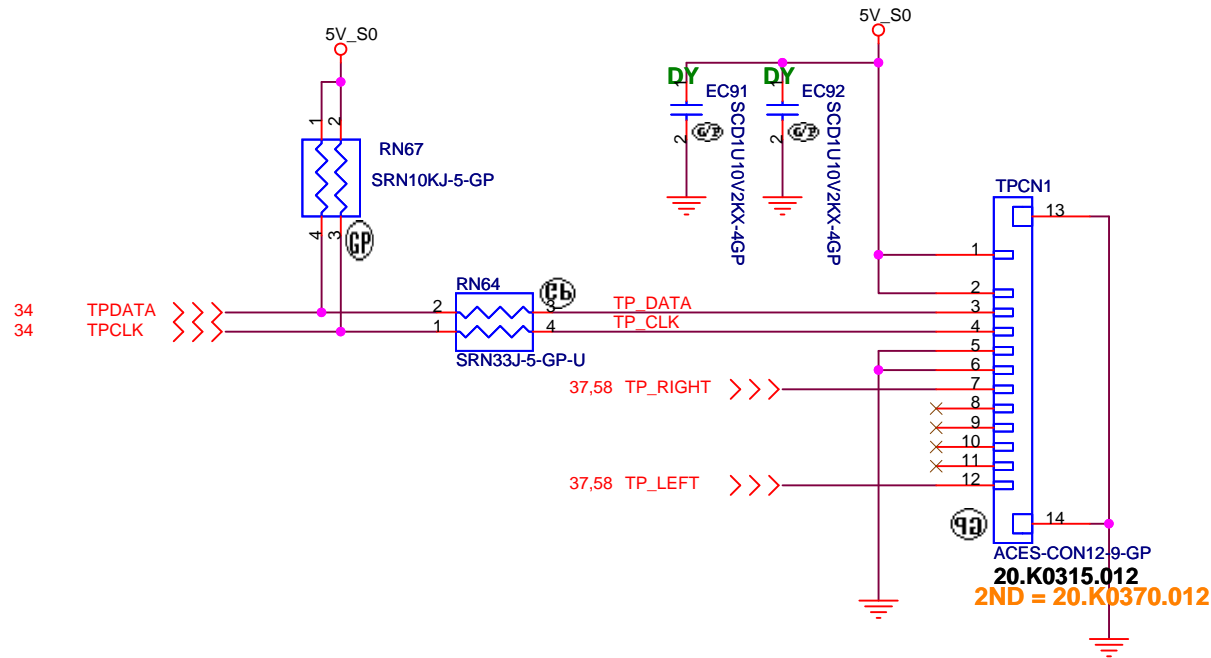


Boot Device must have ID[3:0] = 0000  
Has internal pull-down resistors  
All may be left floated  
FPET7 Elec. P3-46

SJV50

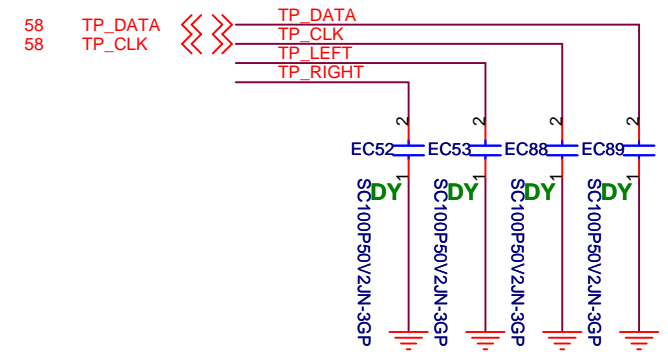
<div>緯創資通</div>		<div>Wistron Corporation</div>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
BIOS			
Size	Document Number		Rev
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# TOUCH PAD



1 12

T/P



SJV50

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Title

TouchPad

Size

Document Number

Rev

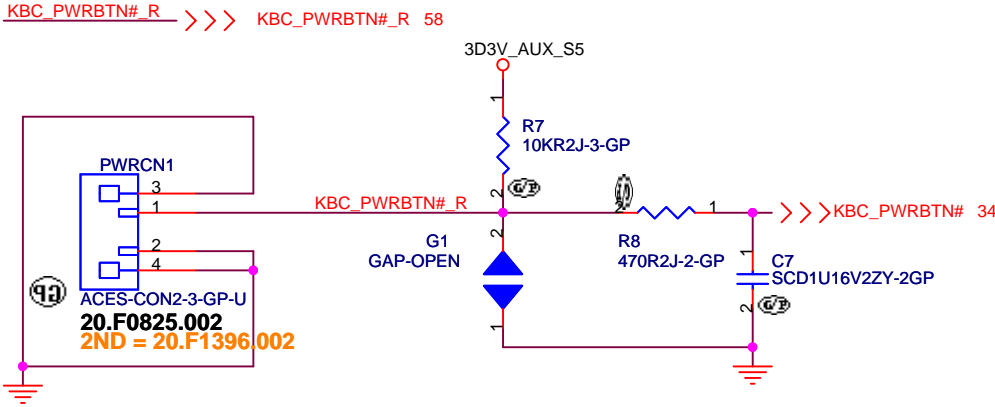
SJV50-PU

-1

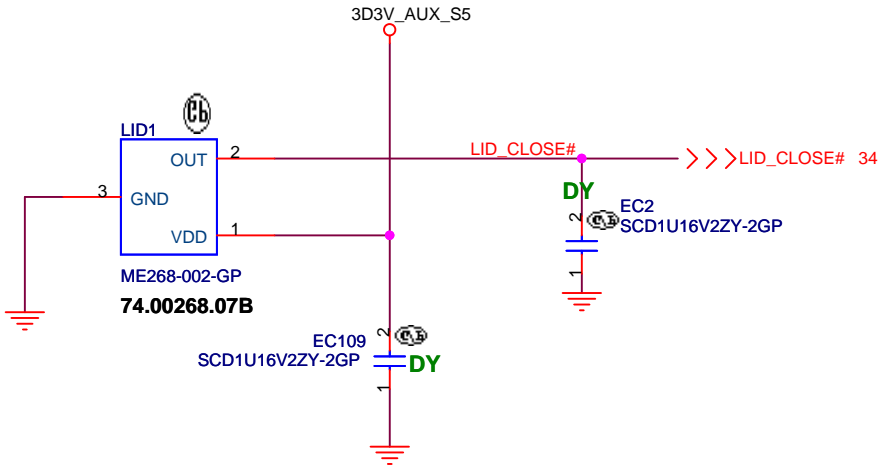
Date: Wednesday, February 25, 2009

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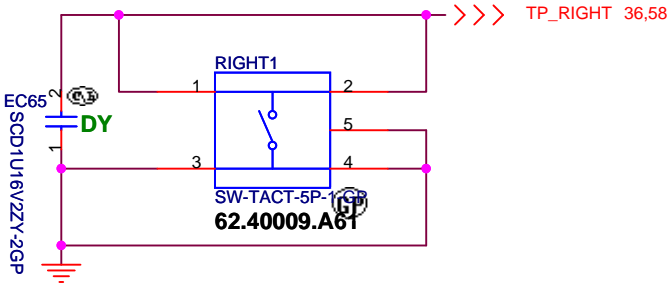
# Power Button Board



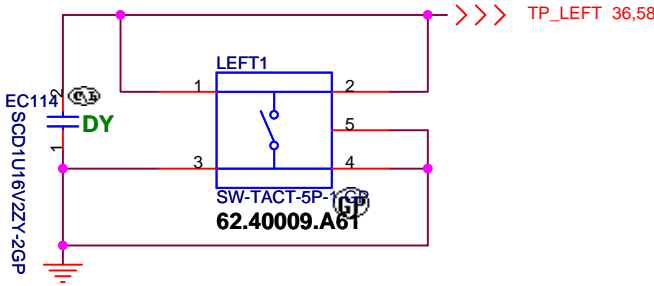
# Cover Up Switch



## RIGHT

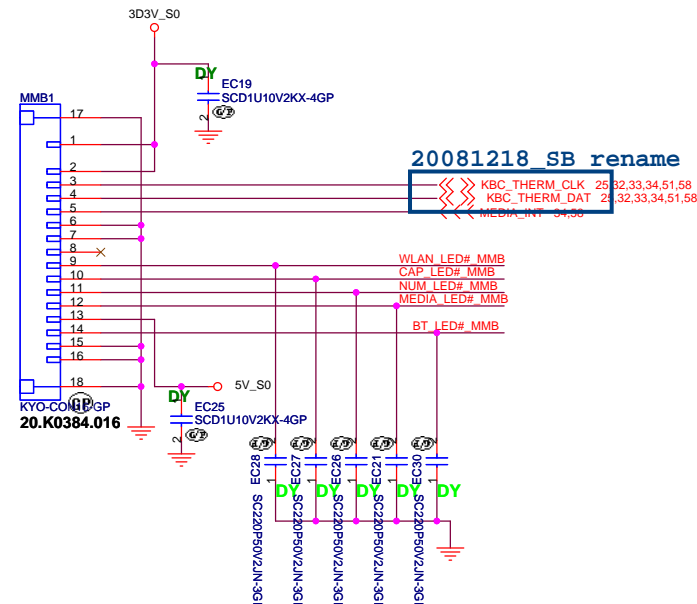
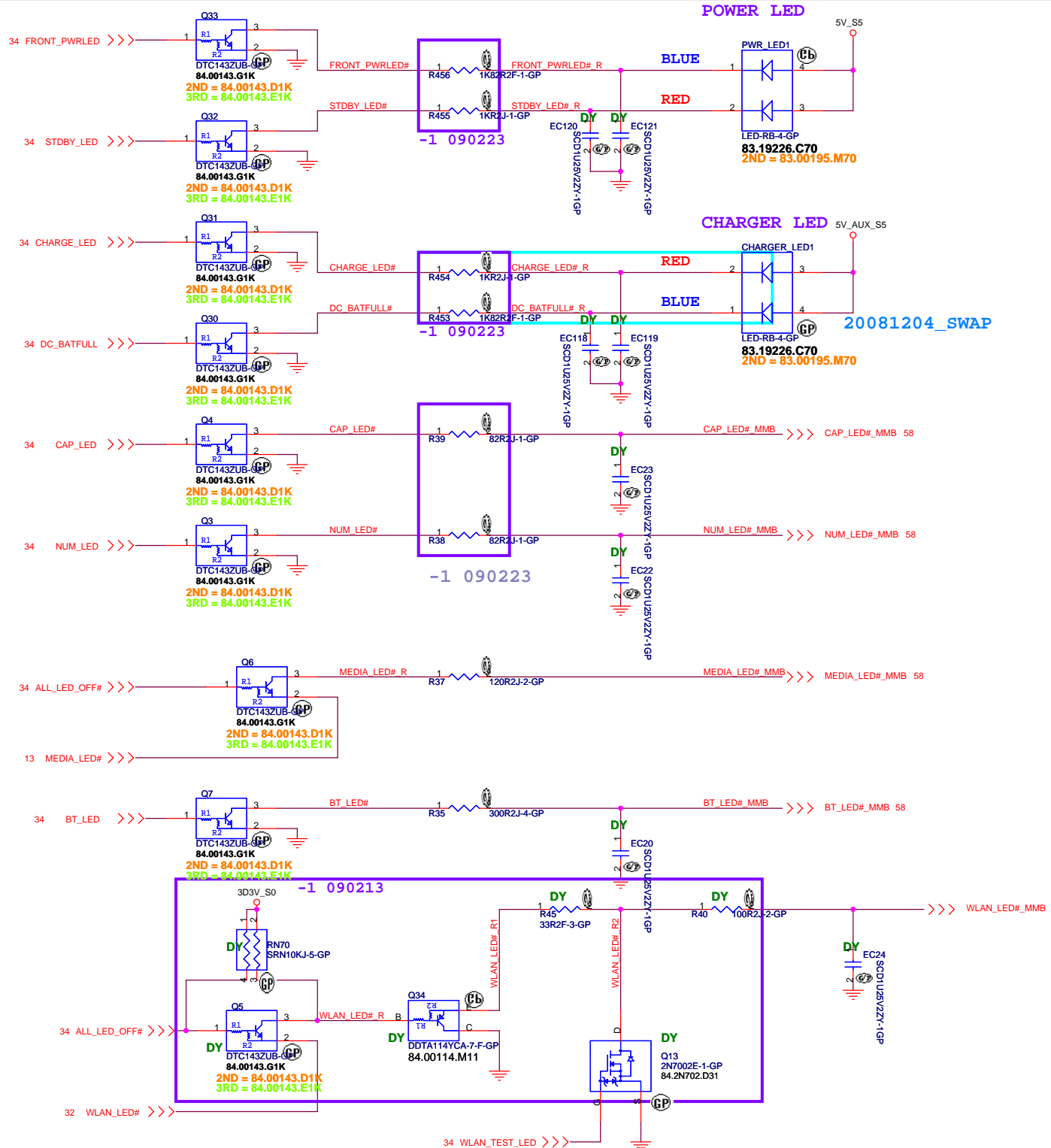


## LEFT

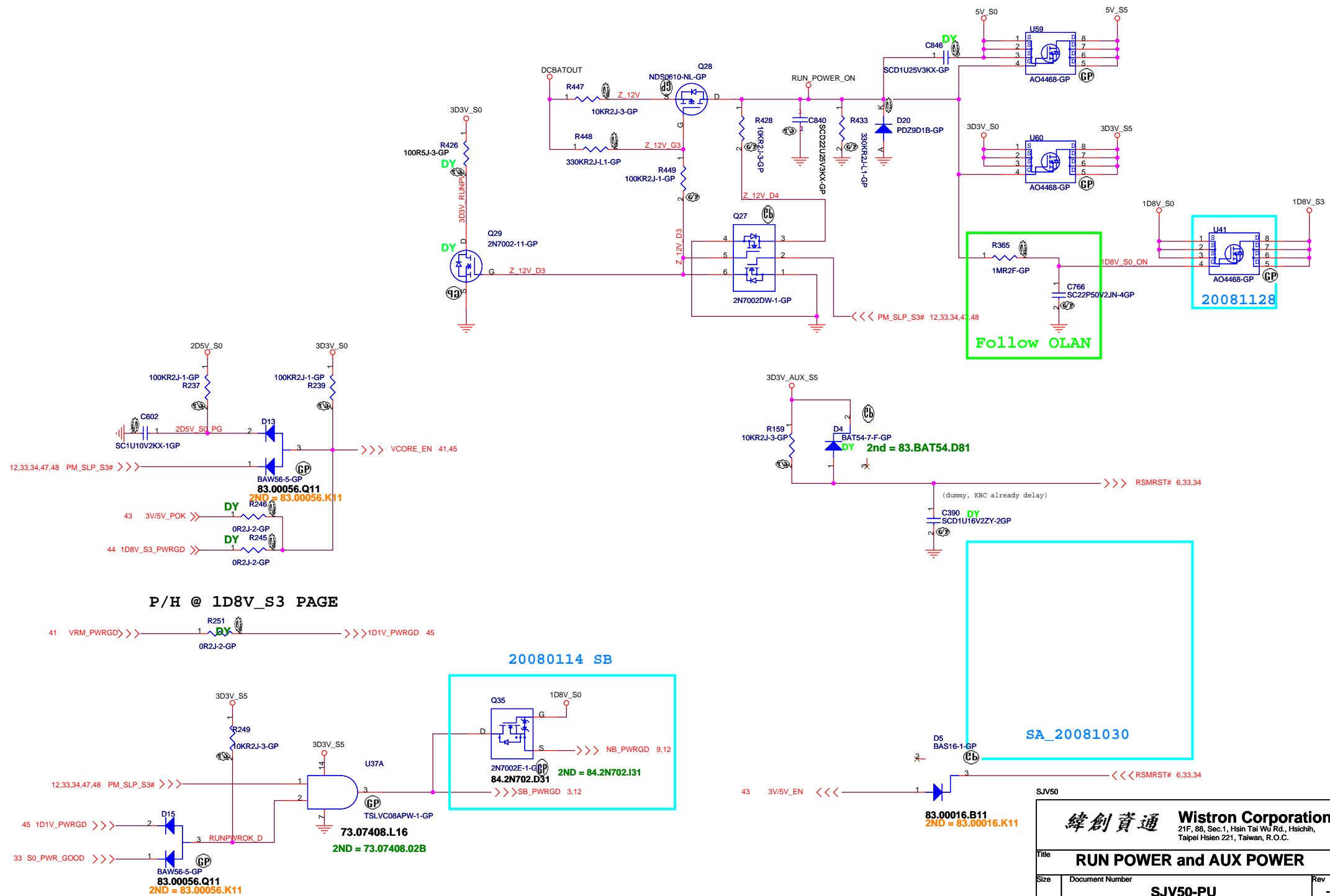


SJV50

<div>緯創資通</div>		<div>Wistron Corporation</div>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<div>Switchs</div>			
Size	Document Number		Rev
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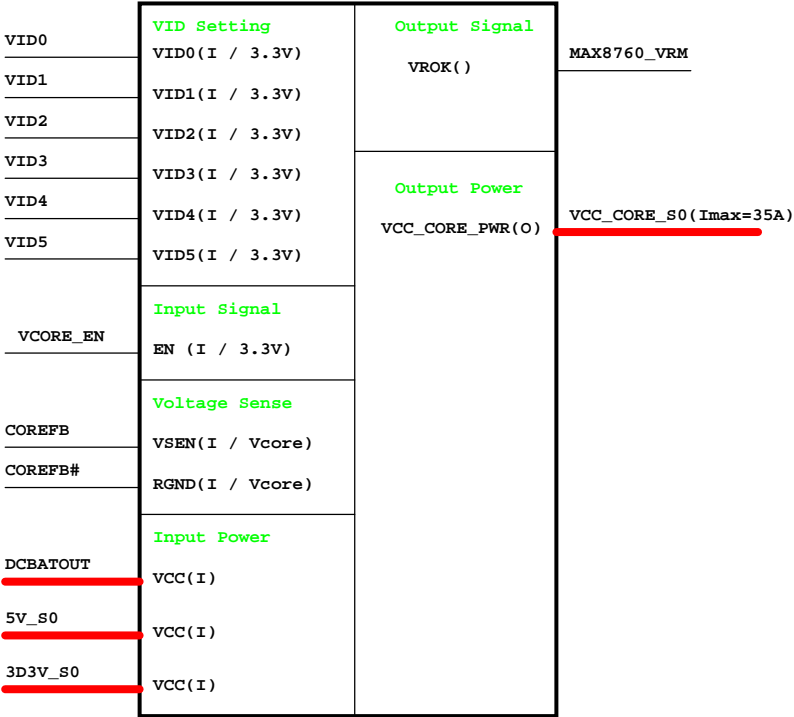


## Run Power

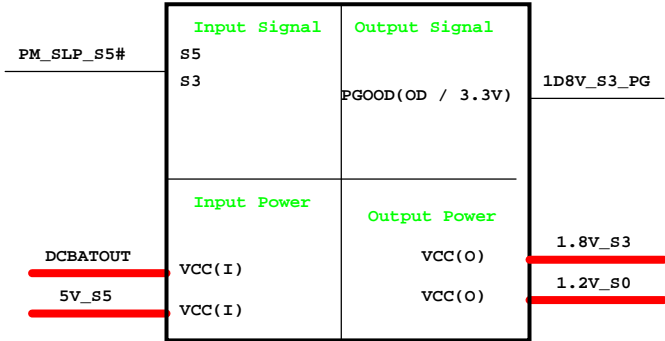




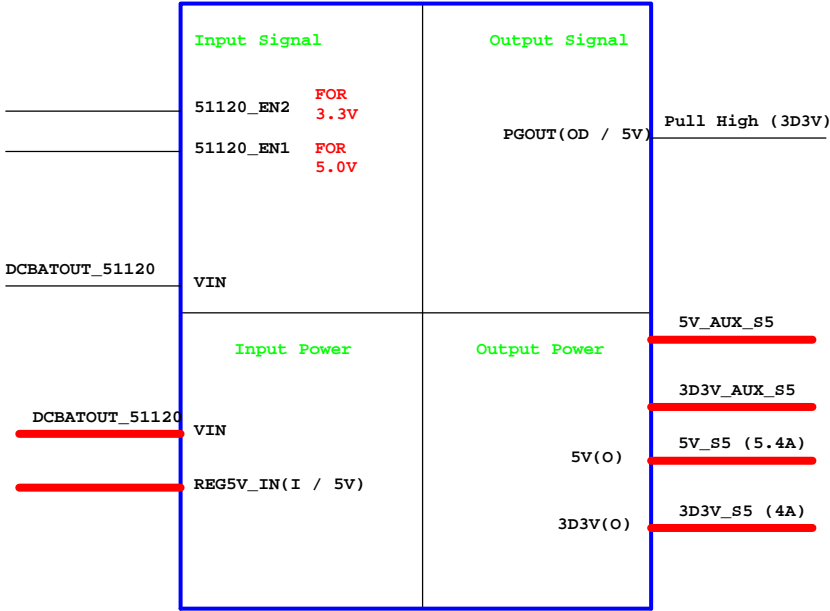
CPU\_CORE  
ISL6264



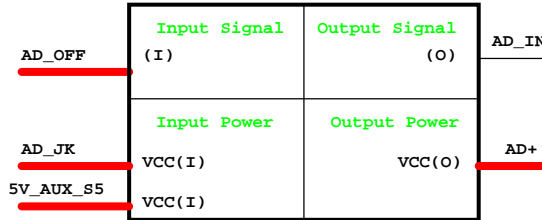
TI TPS51124  
1.8V / 1.2V



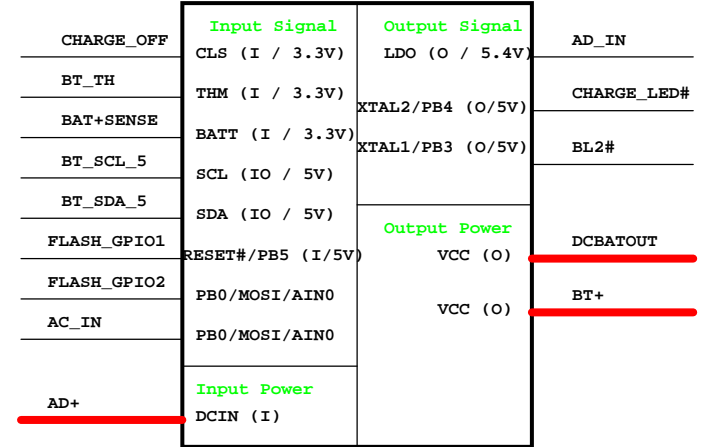
TI TPS51125  
3D3V/5V



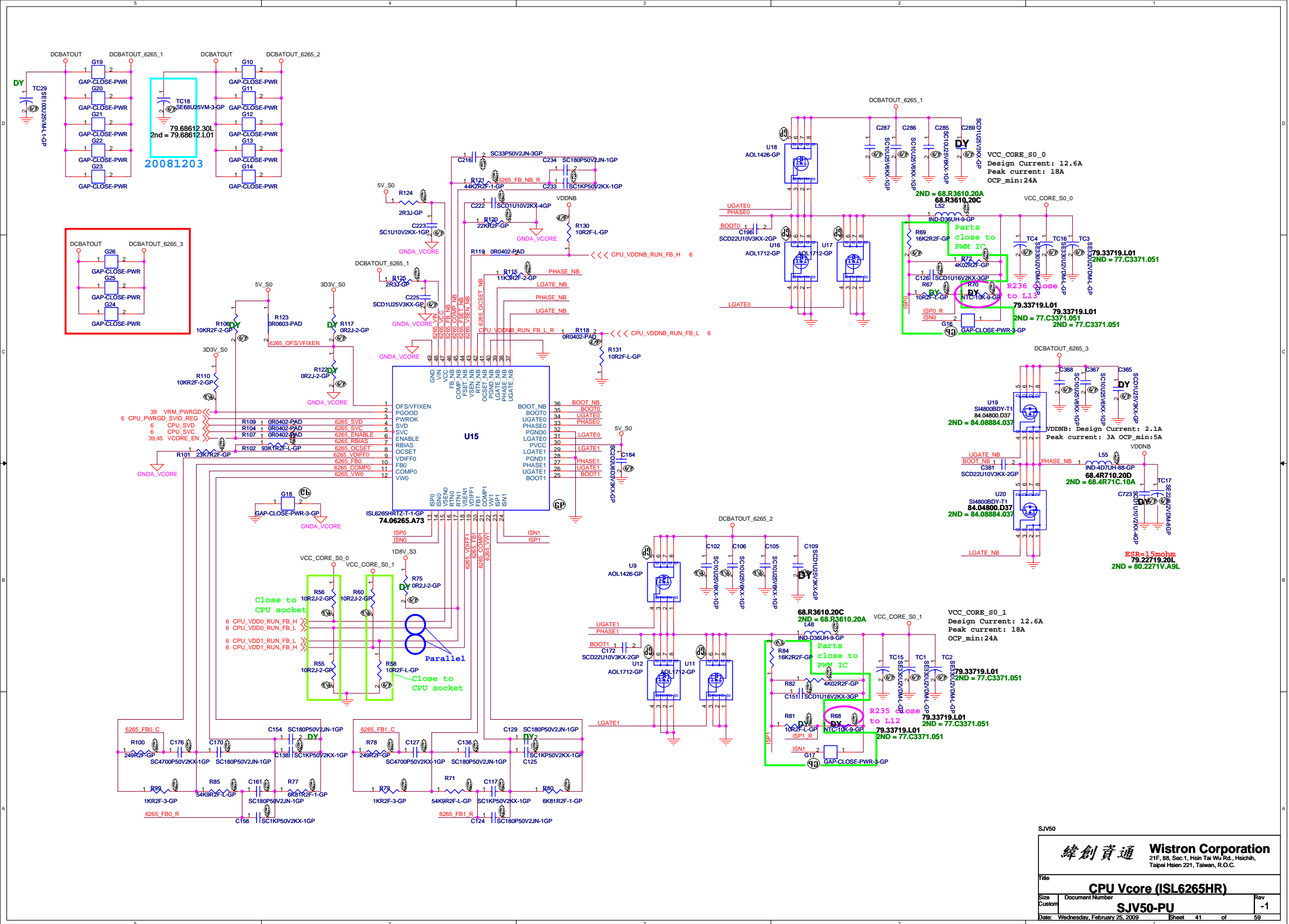
Adapter



Charger\_MAX8731



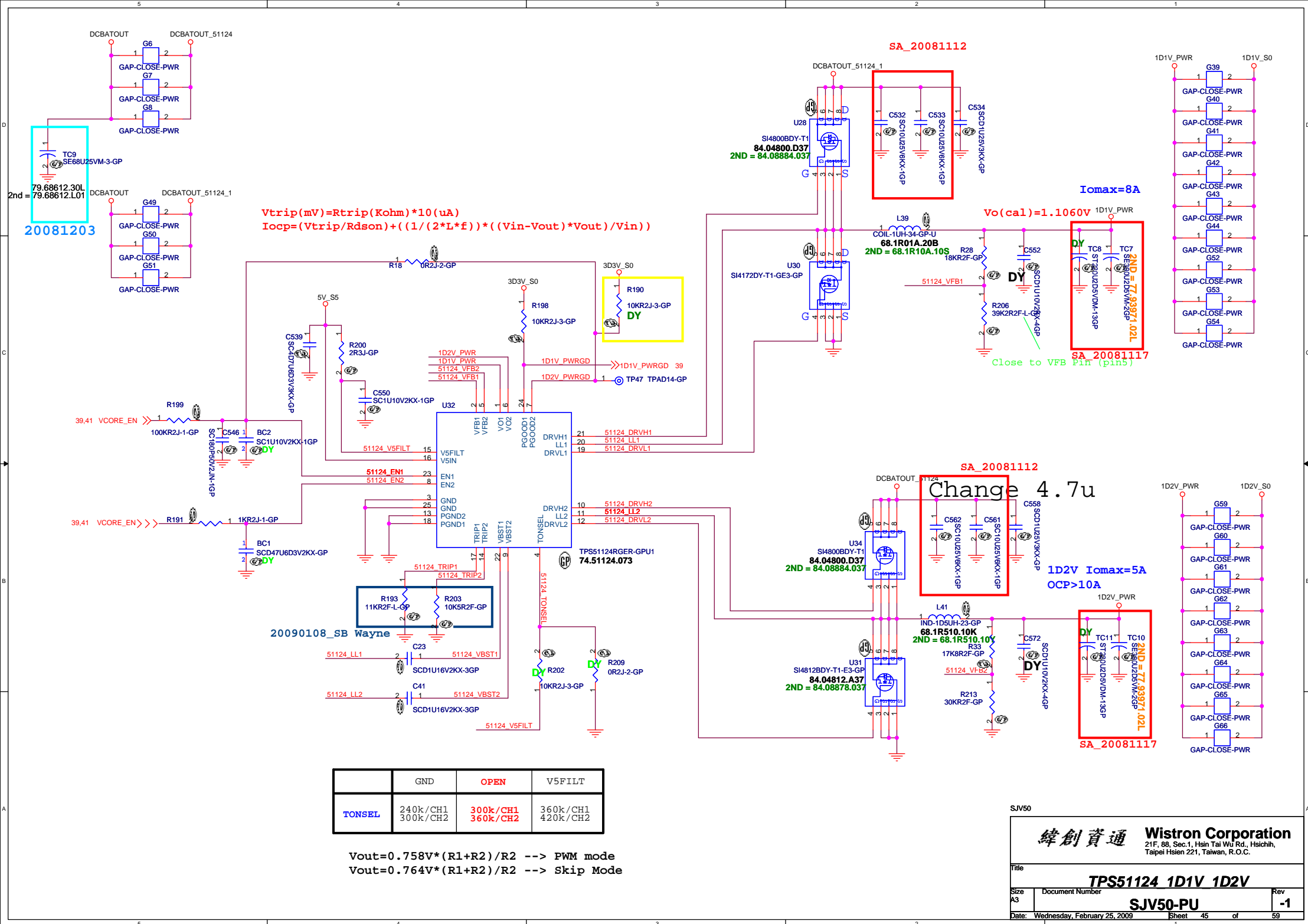
SJV50







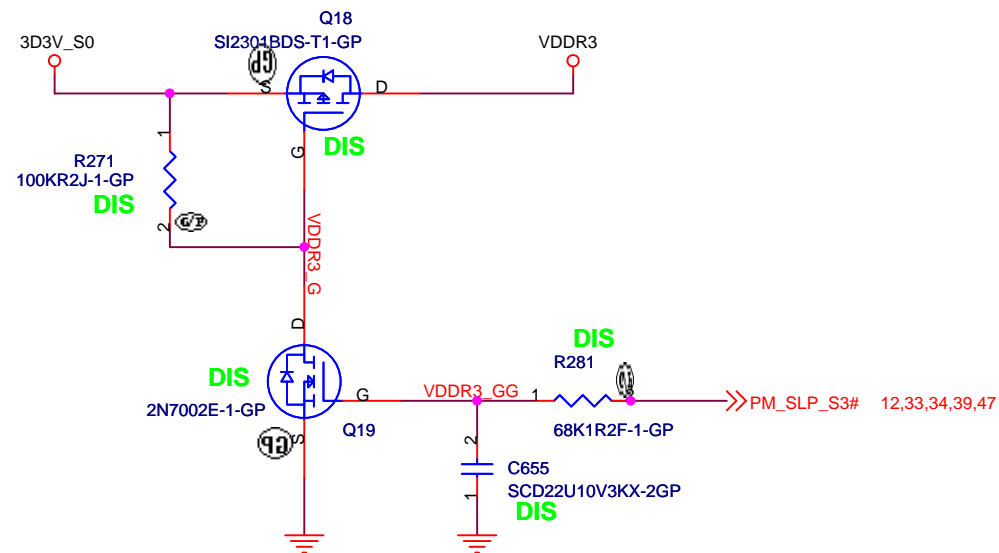












SJV50

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Title

**VDDR3**

Size  
A4

Document Number

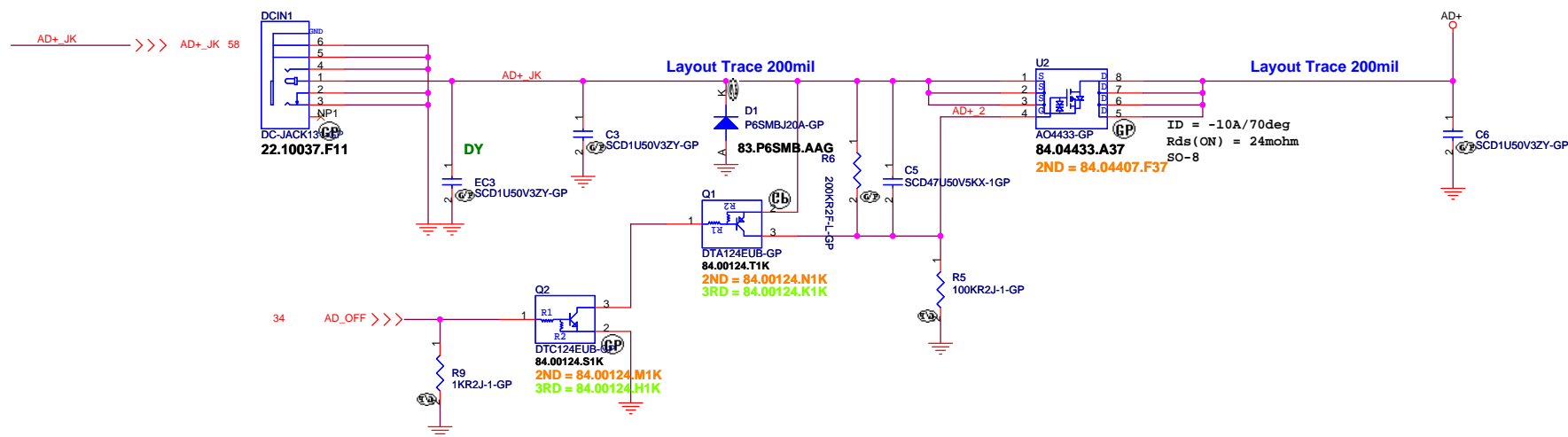
**SJV50-PU**

Rev  
**-1**

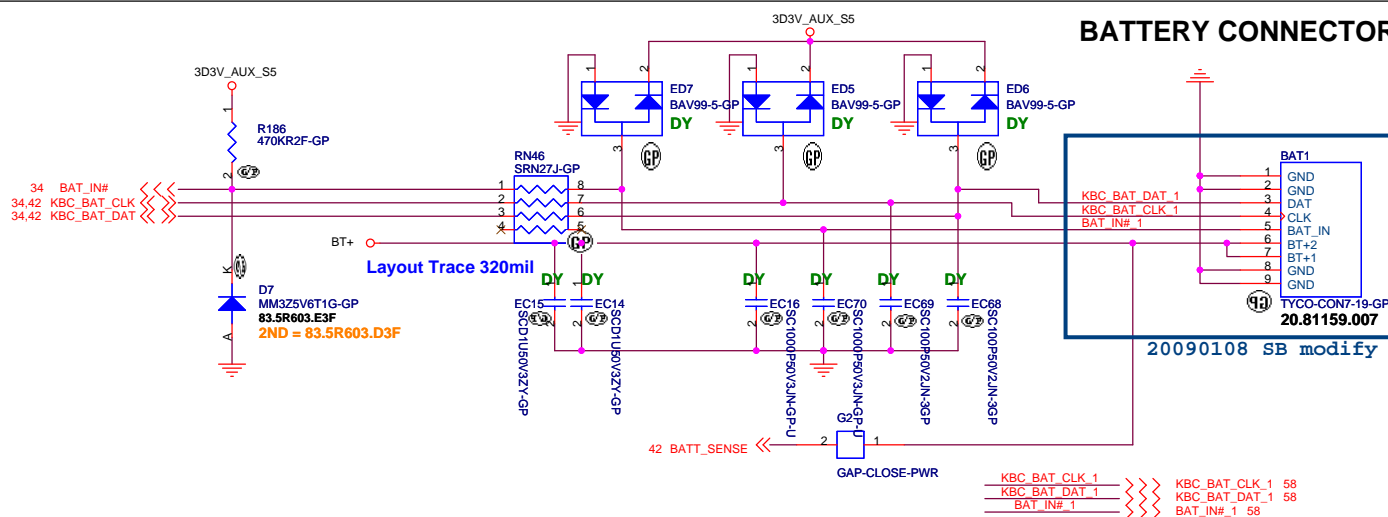
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## Adaptor in to generate DCBATOUT



## BATTERY CONNECTOR

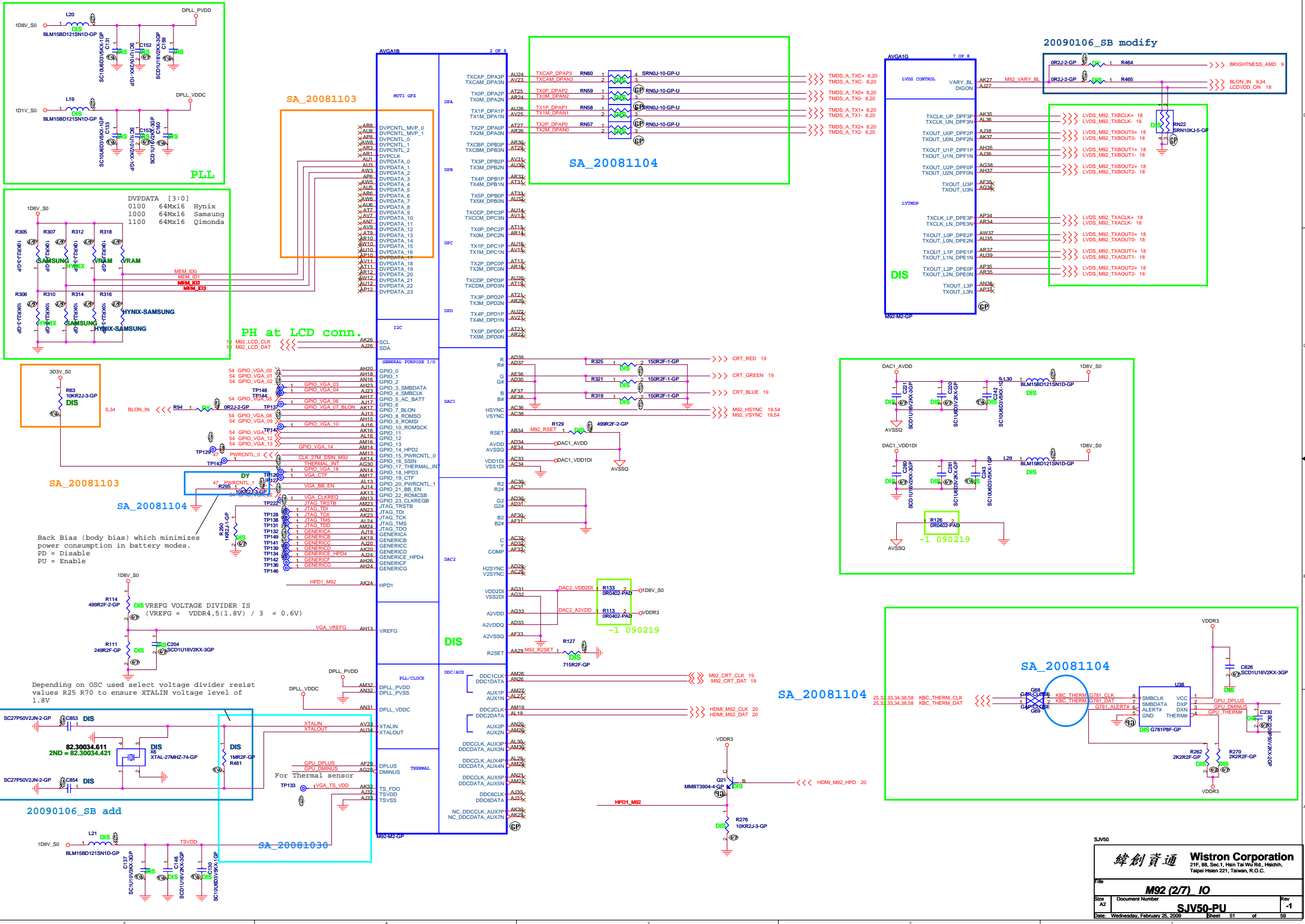


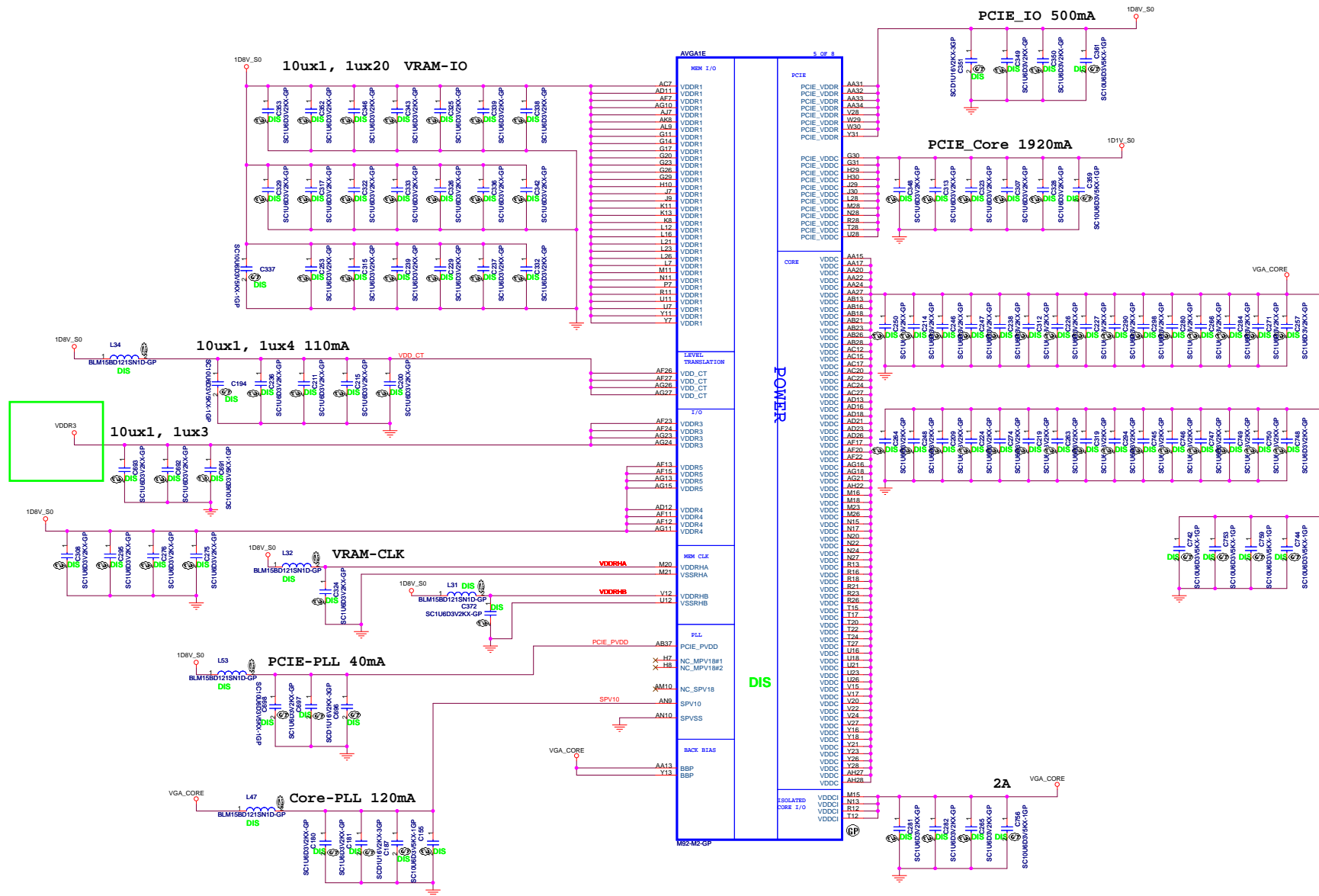
SJV50

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Title			
<b>AD/BATT CONN</b>			
Size	Document Number	Rev	
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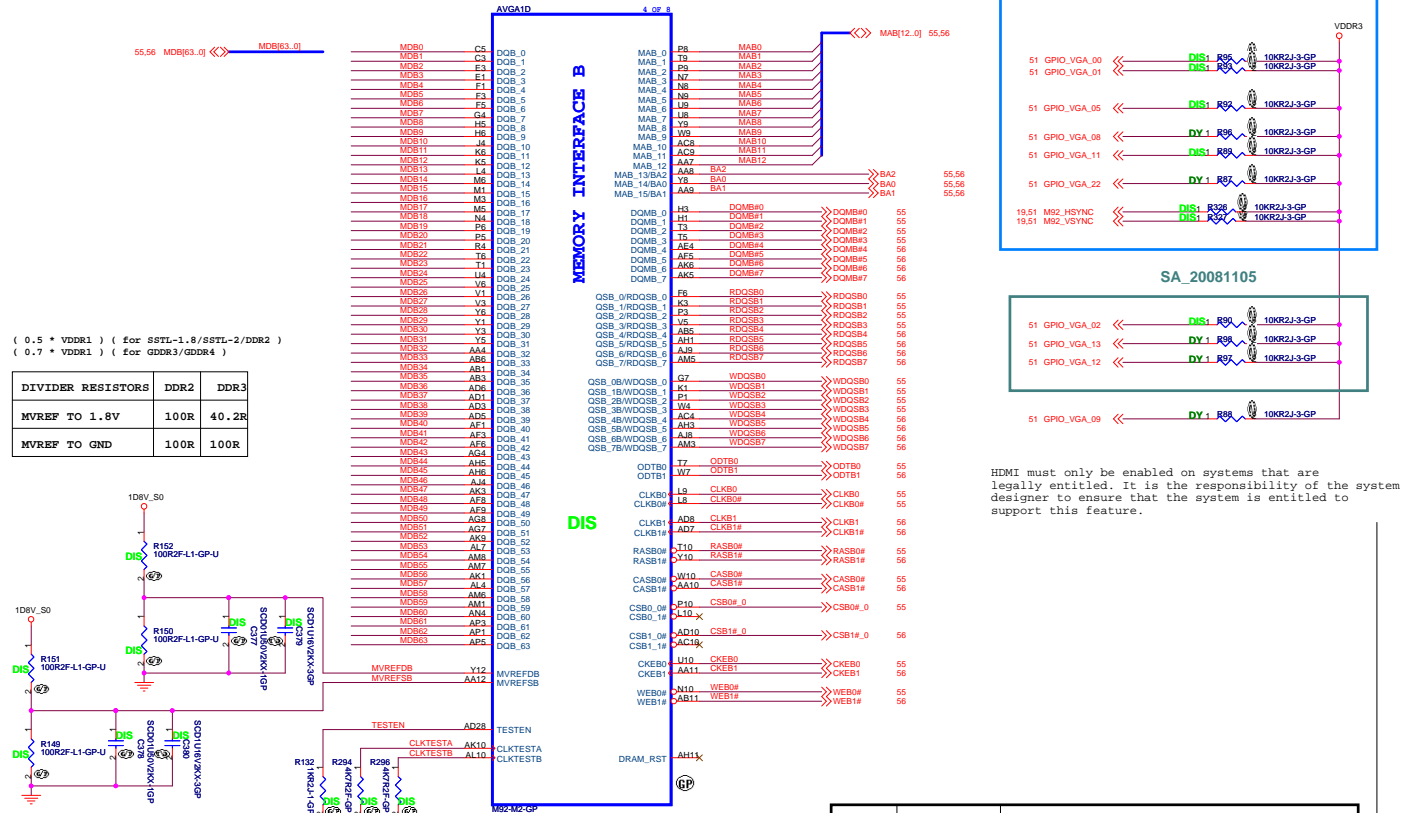




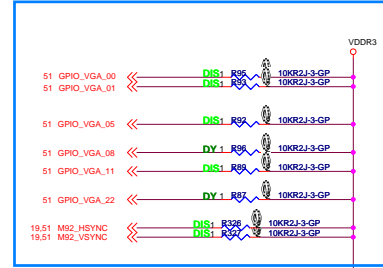




M92-M2 uses memory group B only



SA\_20081104



SA\_20081105



HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.

AMD RESERVED CONFIGURATION STRAPS	
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET	
H2SYNCR, GENERICR	
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET	
GPIO_28_TDO, GPIO21_BB_EN	

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
128MB	x000	ST Microelectronics	M25P05A	0100
256MB	x001		M25P10A	0101
64MB	x010		M25P20	0101
32MB	x		M25P40	0101
512MB	x		M25P80	0101
1GB	x	ChingJis (formerly PMC)	Pm25LV512A	0100
2GB	x		Pm25LV010A	0101
4GB	x			

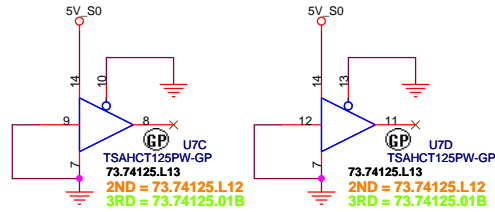
STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING Transmitter Power Savings Enable 0 = 50% Tx output swing 1 = Full Tx output swing	1
TX_DEEMPH_EN	GPIO1	Transmitter De-emphasis Enable 0 = Tx de-emphasis disabled 1 = Tx de-emphasis enabled	1
BIF_GEN2_EN_A	GPIO2	PCIE GEN2 ENABLED 0 = Advertises the PCI-E device as 2.5GT/s 1 = Advertises the PCI-E device as 5GT/s	1
AC_BATT	GPIO5	AC (Performance mode) = 3.3 V Battery saving mode = 0.0 V	
ROMSO	GPIO8	BIF_CLK_PM_EN Serial ROM Output from ROM	0
ROMSI	GPIO9	VGA ENABLED Serial ROM Input to ROM	
ROMIDCFG[3:0]	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT If BIOS_ROM_EN=1, then Config[3:0] defines the ROM type If BIOS_ROM_EN=0, then Config[3:0] defines the primary memory aperture size	x x x
PWRCNTL_[1,0]	GPIO[15,20]	Power control signals to control the core voltage regulator	
BB_EN	GPIO21	Back Bias (body bias) which minimizes power consumption in battery modes. 0V = Disable 3D3V = Enable	0
AUD[1] AUD[0]	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00: No audio function 01: Audio for DisplayPort and HDMI (if adapter is detected) 10: Audio for DisplayPort only 11: Audio for both DisplayPort and HDMI	1
CCBYPASS	GENERICR		0

STRAPS	PIN	DESCRIPTION
GPIO	DVPDATA(23:20) (Internal PD)	Initialization Behavior: This signal is input during reset (no reference clock is required). After reset, the default state is output low (0 V). The signals above can be left unconnected if not used.



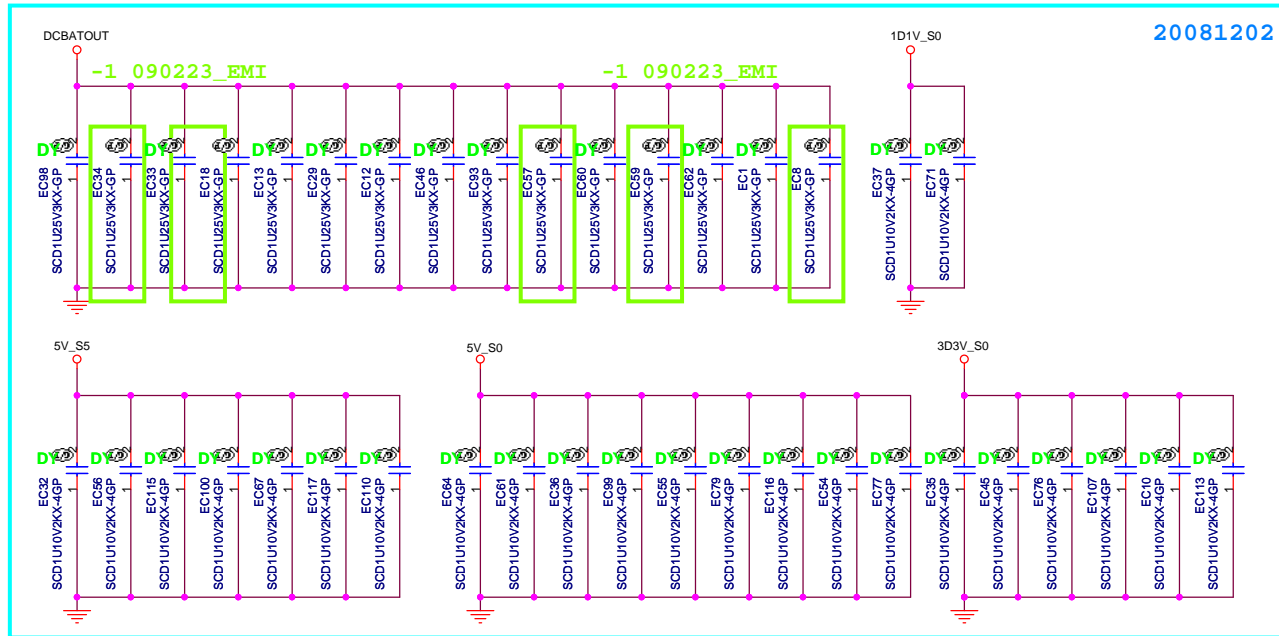
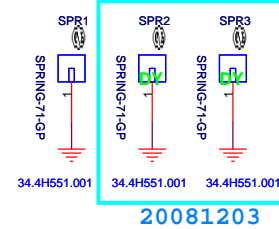
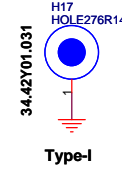
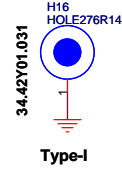
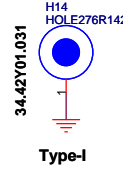
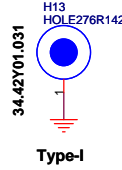
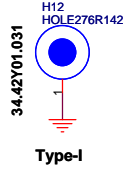
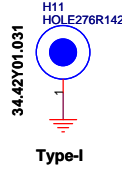
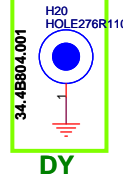
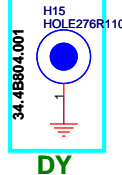
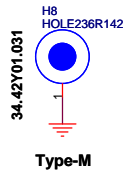
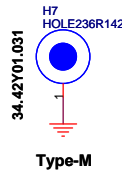
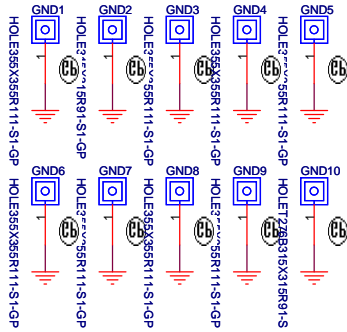






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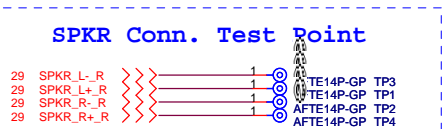
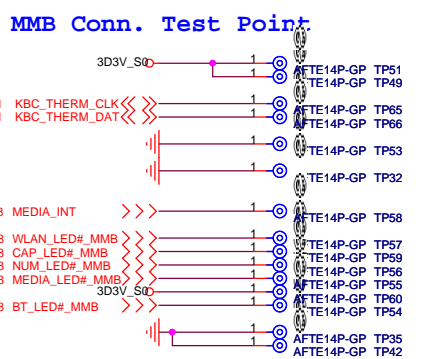
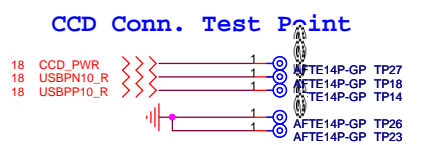
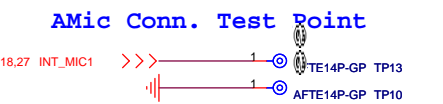
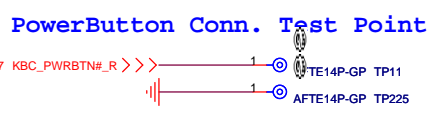
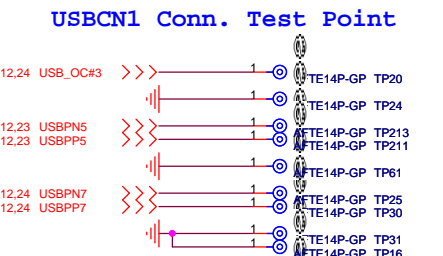
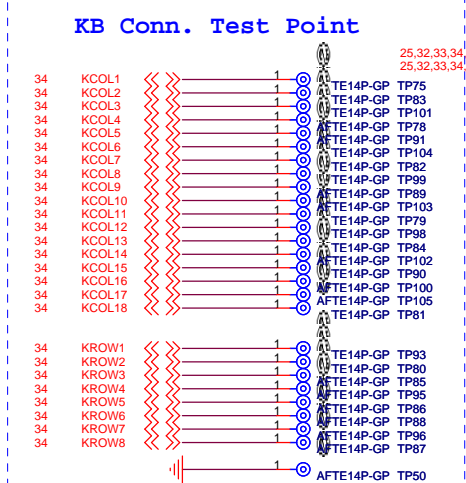
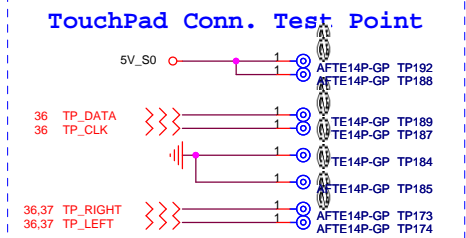
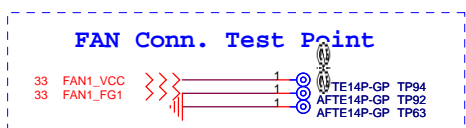
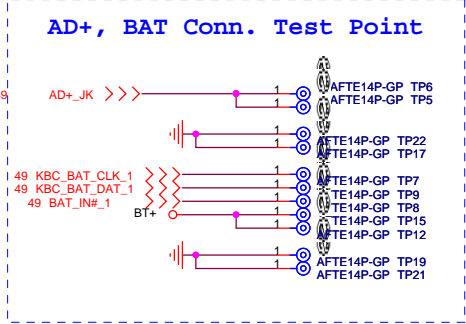
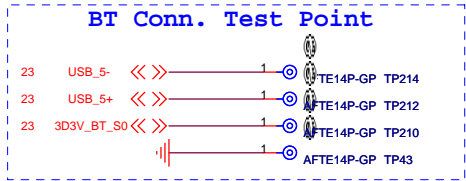
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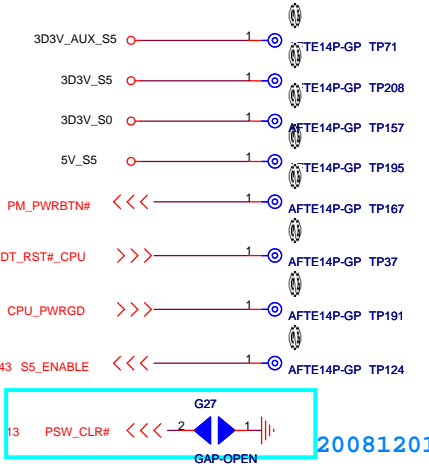
SJV50

緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

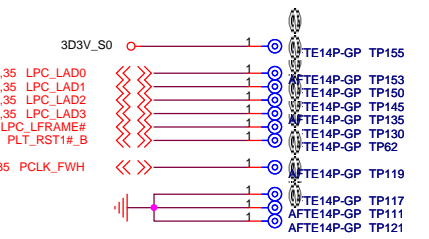
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EMI/Spring/Boss		
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Date: Wednesday, February 25, 2009		
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## Check test point



Test Point放在Dimm Door打開可量測處



5	4	3	2	1
D				
C				
B				
A				

SJV50

<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Change List</b>			
Size	Document Number		Rev
	<b>SJV50-PU</b>		<b>-1</b>
Date:	Wednesday, February 25, 2009		Sheet 59 of 59